

68000

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* Motorola 68020 *

6809-68008-68000-68010

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VOLUME VIII ISSUE VI • Devoted to the 68XX User • June 1986
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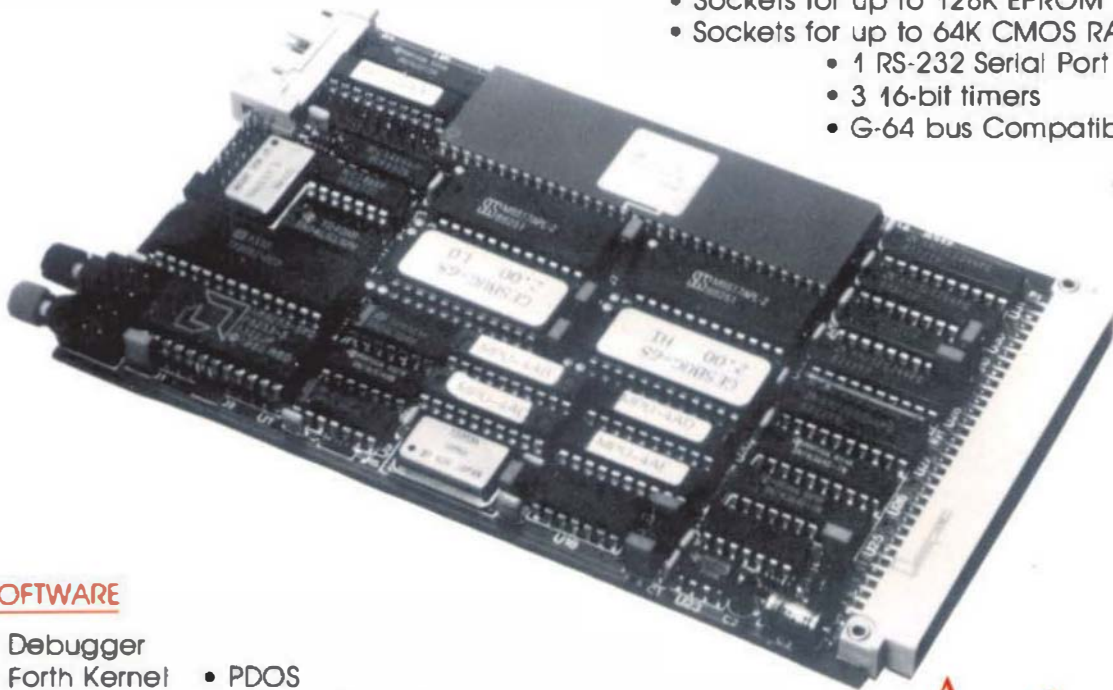
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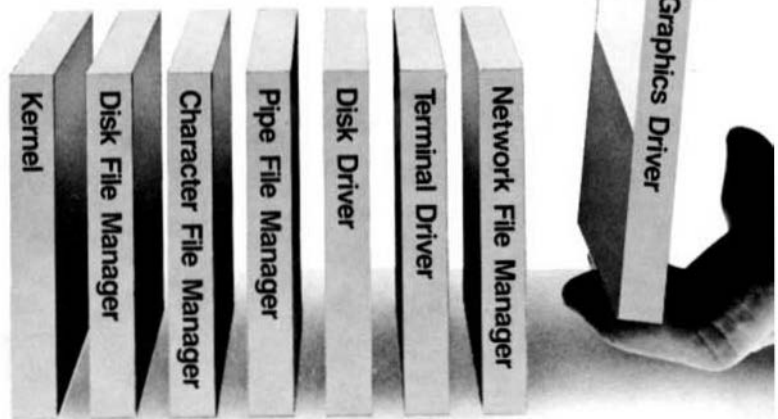
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AT&T 7300 UNIX PC 68010	7.2	4.3
DEC VAX 11/780 UNIX Berkley 4.2	3.6	3.2
DEC VAX 11/750 " " "	5.1	3.2
68000 OS9 68k 8 Mhz	18.0	9.0
68000 " " 10 Mhz	6.5	4.0
MUSTANG-020 68020 MC68881 OS9 16 Mhz	2.2	0.88
MUSTANG-020 68020 MC68881 UNIFLEX " "	1.8	1.22

** Loop: Halo()
{
 register long i;
 for (i=0; i < 999999; ++i);
}

Estimated MIPS - MUSTANG-020 - 2.5 MIPS
Motorola Specs: Burst up to 7 - 8 MIPS - 16 Mhz

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NOTE: 68881 Co-Processor Add \$495.00
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Prices and Specifications subject to change.



THE 6800-6809 BOOKS

..HEAR YE.....HEAR

OS-9™ User Notes

By: Peter Dibble

The publishers of 68' Micro Journal are proud to make available the publication of Peter Dibble's

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FLEX™ USER NOTES

By: Ronald Anderson

The publishers of 68 MICRO JOURNAL are proud to make available the publication of Ron Anderson's **FLEX USER NOTES**, in book form. This popular monthly column has been a regular feature in 68' MICRO JOURNAL SINCE 1979. It has earned the respect of thousands of 68 MICRO JOURNAL readers over the years. In fact, Ron's column has been described as the 'Bible' for 68XX users, by some of the world's leading microprocessor professionals. The most needed and popular 68XX book available. Over the years Ron's column has been one of the most popular in 68 MICRO JOURNAL. And of course 68 MICRO JOURNAL is the most popular 68XX magazine published.

Listed below are a few of the **TEXT** files included in the book and on diskette.

All TEXT files in the book are on the disks.

LOGO C1	File load program to offset memory — ASM PIC
MEMOVE C1	Memory move program — ASM PIC
DUMPC1	Printer dump program — uses LOGO — ASM PIC
SUBTEST C1	Simulation of 6800 code to 6809, show differences — ASM
TERMEM C2	Modem input to disk (or other port input to disk) — ASM
MC2	Output a file to modem (or another port) — ASM
PRINT C3	Parallel (enhanced) printer driver — ASM
MODEM C2	TTL output to CRT and modem (or other port) — ASM
SCPKG C1	Scientific math routines — PASCAL
UC4	Mini-monitor, disk resident, many useful functions — ASM
PRINT C4	Parallel printer driver, without PLAG — ASM
SET C5	Set printer modes — ASM
SETBAS C5	Set printer modes — A-BASIC

NOTE: .C1, .C2, etc. = Chapter 1, Chapter 2, etc.

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Basically OS-9

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BEHIND THE SCENES

I've noticed that many times when a really good movie is at the theaters, there is usually a short release showing how the film was made. You can catch it on a cable station or the PBS network. The film short shows how the special effects were created, how the actors contributed to make the motion picture, and generally what went on behind the scenes. You would think seeing what went on behind scenes would make the motion picture less interesting. But I find (I think most people do) that seeing how it was done, improves my enjoyment of the film. The same can be said of the computer. You can enjoy it as it is, but if you know what goes on BEHIND THE SCENES, you'll enjoy it so much more.

In the April column I talked about the executable memory module. These are the modules that are found in the commands directory, usually CMDS. What makes them different from other files, is not what is in the disk descriptor, but what is in the file. The command module contains three parts--the header, the body and the CRC. We talked a few months ago about the body and CRC of the command module. I also mentioned the the execution offset address and the storage size for the module. These are extensions of the module header. They may not appear in the same in all modules. More about that later.

The first 8 bytes of the module are the header. They give important information about the module and its use. Many systems put this information on the disk, while the program itself tells nothing about its purpose. OS-9 differs from them. The disk file descriptor tells nothing about the modules purpose. The information about the executable module is located at the start of the module. Wherever the module goes, it carries along its own identification. The first 8 bytes are:

Address	Use
\$00,\$01	Sync bytes
\$02,\$03	Module Size
\$04,\$05	Module Name Offset
\$06	Type and Language
\$07	Attributes and Revision
\$08	Header Parity Check

You could add in the Execution offset at \$09,\$0A and the Storage size at \$0B,\$0C. They are extension to the header. For now we'll concentrate on the first 8 bytes.

The Sync Bytes are the first two bytes of the module. They are always \$87 and \$CD. OS-9 uses them to recognize the start of module, hence their name. At start up, OS-9 looks for ROM modules by searching for the sync bytes. What makes them unique is that they don't correspond to any 6809 opcodes. Also, they don't occur in standard ASCII code. So the chances that they would occur except as the sync bytes are pretty remote.

The first 8 bytes of the module are the header. They give important information about the module and its use.... Wherever the module goes, it carries along its own identification.

Next is the module size. Not a whole lot that can be said about it. The two bytes here represent an integer value that tells the size of the module. The system can tell where module ends. And it can use the size to compute the CRC value for comparison to the value in the module.

The Module Name Offset is the number of bytes relative to the module start where the name begins. This is the name that gets placed in the module directory. It uses the system standard for string data. The last character of the name has its 8th bit set high. The modules edition number is placed after the name. It is a byte that indicates what version the module is. It is not necessary to have it there, but it is helpful if you're trying to distinguish between different version of the same module. Run IDENT on a module in the commands directory and it will tell the edition number.

Byte \$06 is the Type and Language Byte. The 4 top bits are the module type. The 4 lower bits are the language indicator. A possible 15 codes can be used for the module type. However, I've only seen 7 used. They are:

Code	Purpose
\$1	Program module
\$2	Subroutine module
\$4	Data module
\$C	System module
\$0	File manager
\$E	Device Driver
\$F	Device Descriptor

\$3 was reserved for a Multi-module, but not yet used, \$5-\$B are user definable. And \$0 is not used. For the language only 4 codes are used. They are:

Code	Purpose
\$0	Data
\$1	Object code
\$2	I-code for Basic09
\$3	P-code for Pascal

Originally, I-code for C Language, Cobol and Fortran were planned, but were never implemented. They would have been \$4 through \$6. Creating a type and language byte is simple. For example, if you created a device driver with your OS-9 assembler, its TYPE/LANG byte would be \$E1. A Basic09 module would be \$22.

The Attribute and Revision Level come next. This byte contains two pieces of information like the previous one. The top 4 bits tell whether the module is reentrant. If the top 4 bits equal \$8 then the module is reentrant or "shareable". A shareable module can be used by a number of users. For example if you are running Basic09 and another user is running it, both of you are using the same module. Only you both have separate data areas. The revision level can range from \$0 to \$F. If two modules are loaded with the same name, the one with the higher revision level will be used. This can be real handy if you want to replace a module that is in memory. OS-9 will always use the highest revision level.

Finally is the Header Check. The first 8 bytes are exclusively ORed together, otherwise know as XOR. To XOR two bytes, each bit is compared in the two bytes. If they match, the result is a 0 and if they differ the result is a 1. For example, let's XOR \$B3 and \$D4. It is easiest to look at the bits.

```
$B3 1 0 0 0 0 0 1 1
$D4 1 1 0 1 0 1 0 0
$57 0 1 0 1 0 1 1 1
```

Notice where that the 8th, 6th, and 4th bits are the same. They yield 0's. The other bits differ between the two numbers, so the are 1. After XORing the first 8 bits the 1's compliment is taken. The result is subtracted from \$FF. The final result is the header check. It is placed in the module header.

TEXT COMPRESSION

This month's programs deal with text compression. I wrote these two programs last year while trying to develop a method putting files on a disk with the least amount of space. With the advent of cheap memory and lower cost storage, text compression is not as important as it was at one time. But it can still be fun to play with it.

There are a number of methods to reduce text size. One method is to use a table of common words. Normally ASCII text uses only the first 128 bytes. These include bytes \$00 thru \$7F. The 8th bit never is set. Setting the 8th bit could be used to signal that the word should be looked up in the table. This would only account for 128 common words using byte \$80 thru \$FF. The processor could also extend the table and automatically use the next byte in line to access a table of 32768 words. That is quite a large table of common words. Most of the dictionaries I have seen for spell checkers aren't that large. The dictionaries size would have to be only perhaps 1000 words to cover most commonly used words. One letter words would not be in it. There is no sense in storing one byte words in two bytes. Two letter words would become a break even deal. Anything more would be a savings. This method is used. Many Basic languages tokenize keywords. A one or two byte token is used to represent a keyword in the language. The net result is reduced code size. The draw back to such a system is the overhead. Our table of common words would need a large storage area. Therefore, its savings in memory would not be realized until we started using texts or files that exceeded the table size and tokenized words.

Another method is to put more code in the allotted space. A byte is used to store one character. The code used is ASCII. It represents all printable and non-printable characters. Two bytes makes an integer which can hold two characters. What if we could put more in it? Imagine a character set shorter than the ASCII set. A very minimal set could be A thru Z, 0 thru 9, three punctuation and a carriage return character. This set comprises 40 characters in all. This method is called radix 40. Three characters are stored in the integer with the following formula:

$$((c1*40)+c2)*40+c3$$

C1, c2 and c3 are now in the integer form. To remove them the process is reversed. The savings is 50% in text space. The disadvantages is a narrow character set. There are no lowercase letters and only a few punctuation

are permitted. This would definitely limit what kind of text you could create.

The method I used in this month's programs retains the full ASCII character set, while being easily implemented. Only 7 bits are used in the byte to store ASCII code. Normally the 8th bit is left unused. This location could be used to hide something. The most often occurring character in standard text is the space. If the space could be eliminated from the text file, there should be a considerable savings of space. The method used by PACK is to read a character from the standard input. If it is a space, set a flag. Then it reads another character. If the space flag is set, the 8th bit on the next character is set high and that character is written to the standard output path. Otherwise the character is written as it is read. The UNPACK program reads a packed file and restores it to its original form. If the character has its 8th bit set high, a space is put on the output path and then the character is written with the 8th bit cleared. If the 8th bit is not set, it is written as it was read.

Besides having fun with PACK and UNPACK, they give us a good example of how the module header is created. The MOD command in the source code is very important. In PACK, it reads:

```
MOD PACEND, NAME, $11, $B1, START, PACKEM
```

It helps to create the module header. Here's how it works. The first two bytes of the header are \$B7 and \$CD. The next two are the size, which is equal to PACEND. Next two are the offset to the name which is equal to NAME in the MOD list. Module type/language type is \$11, program module and object code. Attributes/Revision level is \$B1, shareable and revision 1. Check the tables I gave earlier for these two bytes. START is the execution offset and PACKEM is the permanent storage requirement. Once you've written and compiled PACK, use DUMP to examine the module header and see what is in the header. Also try analyzing the UNPACK module.

The MOD code can specify header information for other type of modules, too. Normally the last two arguments specify the entry point and data memory size. But they can vary with the module type. A subroutine module will have its last argument set to 0, since it will use the caller's memory. A device descriptor will use the last two positions in MOD to indicate where the file manager's name and driver's name are located in the module. The data module will indicate the data start and the data size. So, depending on the module, a number of different pieces of information can be conveyed with the module header extensions.

The best thing to do is to examine things for yourself. Use IDENT to look at the different modules. Also, DUMP the module to your printer and examine the first 8 bytes or so. It's fun to watch a good show. It is more fun to go BEHIND THE SCENES.

```
00001 *****
00002 * PACK by Ron Voigtis
00003 * 2-FEB-86
00004 *
00005 * This program will pack an ascii file
00006 * into a compact file by hiding
00007 * spaces.
00008 *
00009 * Usage: pack (infile)outfile
00010 *
00011 *          naa  PACK
00012 *          tti  packs ascii files
00013 *
00014 * Note: a USE /DB/DEFS/OS90DEFS
00015 *       is between the IFP and
00016 *       ENDC statements.
00017 *          IFP:
00018 *          ENDC
00019 *
00020 *
00021 * Equates
00022 0001  BUF$12  equ 1          Buffer size
```



```

00023 0001      STDOUT equ 1      Standard output path
00024 0000      STDIN  equ 0      Standard input path
00025          *
00026          * Data section
00027 0 0000      org 0
00028 0 0000      CHAR   rmb 1      the buffer
00029 0 0001      SFLAG   rmb 1      Space detect flag
00030 0 0002      rmb 200      save some stack space
00031 0 00C9      STACK   equ -1
00032 0 00CA      PACMEN   equ *
00033          *
00034          *
00035          * program section
00036 0000 07C0005b    and PACEND, NAME, $11, $01, START, PACMEN
00037 0000 506163EB    NAME   FCS   "Pack"      Name of the module
00038 0011 01          EDITION fcb 1      Edition number
00039          *
00040 0012          START   equ *
00041 0012 6F41      cir     SFLAG,U      clear space flag
00042          *
00043          * Read from STDIN a CHAR
00044 0014 8600      READCH  lda  STDOUT      Get from standard output
00045 0016 30C4      leax  CHAR,U          a character
00046 0018 108E0001    ldy  @BUFSIZ      one byte at a time
00047 001C 103F89      os9  lsrwrd      using the D59 Read
00048 001F 2529      bcs  ERRCHK      If carry is set, branch to err
00049          *
00050          * Check SFLAG
00051 0021 6D41      CMFLAG 1st  SFLAG,U      Is flag set?
00052 0023 270A      beq  CHSPAC      No, then check for a space
00053 0025 A6C4      lda  WIDESP      Otherwise get character
00054 0027 8A00      ora  #000      Set the MSB high
00055 0029 A7C4      sla  CHAR,U          to hide a previous space
00056 002B 6F41      cir     SFLAG,U      and save it
00057 002D 200C      bra  WRITCH      Write the new character
00058          *
00059          * Write character or set SFLAG
00060 002F A600001F    CHSPAC  lda  SPACE,PCR      Get a space
00061 0033 A1C4      cmpa  CHAR,U          and compare it the character
00062 0035 2604      bne  WRITCH      If not a space, write it
00063 0037 6341      com  SFLAG,U          Otherwise set the flag
00064 0039 2009      bra  READCH      and read another character
00065          *
00066          * Write the current character al CHAR
00067 003B 8601      WRITCH  lda  STDOUT      Get the standard output
00068 003D 30C4      leax  CHAR,U          and the character
00069 003F 108E0001    ldy  @BUFSIZ      which is on byte long
00070 0041 103F8A      os9  lsrwrd      and write it
00071 0046 2502      bcs  ERRCHK      If carry set go to ERRCHK
00072 004B 20C4      bra  READCH      Otherwise read another one
00073          *
00074          * Finish up the program
00075 004A C1D3      ERRCHK  cmob BZ11      Is this an end-of-file?
00076 004C 2601      bne  DONE      No, then return with error
00077 004E 5F      clrb      Otherwise clear the error
00078 004F 103F86      os9  Fbcrlt      and go back
00079          *
00080 0052 20          SPACE  fcc  / /      This is the space
00081          *
00082 0053 C20609      end
00083 005b          PACEND   equ *
00084          end

00000 error(s)
00000 warning(s)
00056 00006 program bytes generated
000CA 00202 data bytes allocated
01EE8 07912 bytes used for symbols

```

```

00089          * Usage: unpack (infile) outfile
00090          *
00091          nam  UNPACK
00092          tti  Unpacks "packed" files
00093          *
00094          * Note: a USE /DB/DEFS/OS9DEFS
00095          * is between the IFPI and
00096          * ENDC statements.
00097          IFPI
00098          ENDC
00099          *
00100          * data section
00101 0001          BUFSIZ  equ 1      buffer size
00102 0001          STDOUT  equ 1      Output path
00103 0000          STDIN   equ 0      Input path
00104          org 0
00105 0 0000          CHAR   rmb 1      the buffer
00106 0 0001          SFLAG   rmb 1      Space flag
00107 0 0002          rmb 200      Stack space
00108 0 00C9          STACK   equ -1
00109 0 00CA          PACMEN   equ *
00110          *
00111          * Program section
00112 0000 07C0005b    and UEND,NAME,$11,$01,START,UMEN
00113 0000 556E7061    NAME   FCS   "Unpack"
00114 0013          START   equ *
00115          *
00116          * Characters are read into CHAR
00117          * If an error occurs execution
00118          * goes to ERRCHK
00119 0014 8600      READCH  lda  STDOUT      Get standard input
00120 0016 30C4      leax  CHAR,U          Point to character buffer
00121 0018 108E0001    ldy  @BUFSIZ      Get buffer size
00122 001C 103F89      os9  lsrwrd      Do a read
00123 001F 252A      bcs  ERRCHK      Check error if carry set
00124          *
00125          * Check bit 7 on CHAR
00126          * If it's set a space goes before the
00127          * the character and bit 7 is cleared
00128 0020 8600      CHKBIT  lda  BZ10000000      Get bit mask
00129 0022 A4C4      anda  CHAR,U          AND it with the buffer
00130 0024 2715      beq  WRITCH      If zero write it
00131 0026 867F      lda  BZ01111111      else get mask and
00132 0028 A4C4      anda  CHAR,U          AND it with buffer
00133 002A A7C4      sla  CHAR,U          to remove reset 8th bit
00134          *
00135          * output a space if bit 7 is set
00136 002C 8601      SPCOUT  lda  STDOUT      Get standard output
00137 002E 30000020    leax  SPACE,PCR      Get space character
00138 0030 01          ldy  #1      Ready for one character
00139 0032 108E0001    os9  lsrwrd      and write it!
00140 0034 103F8A      bcs  ERRCHK      Go to error if carry set
00141 0036 250F      bra  ERRCHK      Go to error if carry set
00142          *
00143          * Output CHAR
00144 0038 8601      WRITCH  lda  STDOUT      Get standard output path
00145 003A 30C4      leax  CHAR,U          Get buffer
00146 003C 108E0001    ldy  @BUFSIZ      Ready for one character
00147 003E 103F8A      os9  lsrwrd      and write it!
00148 0040 2502      bcs  ERRCHK      Go to error if carry set
00149 0042 20C9      bra  READCH      Go read another character
00150          *
00151          * Check for end-of-file
00152          * Anything else is a read error
00153 0044 C1D3      ERRCHK  cmob #leof      End of file?
00154 0046 2601      bne  DONE      No, then finish up
00155 0048 5F      clrb      Yes, return without error
00156 004A 103F86      os9  Fbcrlt      Return
00157          *
00158          * The space
00159 0052 20          SPACE  fcc  / /      A space!
00160          *
00161 0053 6A9613      end
00162 005b          UEND     equ *
00163          end

00000 error(s)
00000 warning(s)
00056 00006 program bytes generated
000CA 00202 data bytes allocated
01EE8 07882 bytes used for symbols

```


"C"

User Notes

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INTRODUCTION

This chapter provides information on recent updates to the C compilers for the 6809 and 68000. It also presents a one-screen editor written using the curses library functions.

C COMPILER UPDATES

Both Windrush and Microware released new versions of their C compilers, with Windrush C being for 6809 Flex and Microware C being for OS/9-68000. Introl notified its dealers that its 6809 OS/9 C compiler will be marketed only for Level 2, due to insufficient memory to run it on Level 1 systems.

Windrush (McCoah) C compiler version 27.0:0 has been released and has several significant improvements over previous versions.

The compiler will now run with a MEMEND less than \$BFFF. This was accomplished by making the CPASS1.CMD of the compiler somewhat smaller and removing the check in CC.CMD for a MEMEND of \$BFFF which was inserted in version 26, but which caused the compiler to be only marginally useful on many FLEX systems. Produced object programs will now ensure that the last address is less than the current MEMEND, to help prevent system crashes due to too-large programs.

The C pre-processor, CPREP.CMD, has been rewritten. It allows macro definitions and strings to be continued from one line to the next by preceding the intervening carriage return with a back-slash, as specified in K & R. It does its own error processing, rather than letting CPASS1.CMD flag errors in the input program, and occasionally miss them. It supports nested comments, a common extension to K & R. It detects and flags recursive macro definitions, rather than looping until it depletes its stack space.

The library routines have been corrected in several areas. Since the FLEX 1.CMD routine reverts to terminal input upon reaching the end of its input file, the user needs some manner to indicate end of file. This previously was done by entering a control-D, but version 26 of the compiler deleted this capability. Version 27 reinstates this capability. The FLEX 0.CMD, P.CMD, and smaller output filter commands were not processed correctly in version 26, mistakenly maintaining terminal parameters such as width and depth on these pseudo output files. This has been corrected in version 27.

Both Windrush and Microware released new versions of their C compilers....

Windrush version 27.0:0 has several significant improvements over previous versions....

The C pre-processor, has been rewritten....

The library routines have been corrected in several areas....

A major enhancement introduced in version 27 is standard I/O redirection using the MSDOS, OS/9, UNIFLEX, and UNIX notation of "<filename" for input file and ">filename" for output file. This enhancement also corrects the problem described in an earlier chapter pertaining to the incorrect handling of quoted strings on command lines. Since this increased complexity costs a significant amount of code in the library routines, it is effective only when the user includes a dummy call to rio-init() somewhere in the C program, in a manner similar to the use of dummy calls to pflinit() or pffinit() for printf().

A known remaining problem with the McCoah family of C compilers involves the linking of variables across separately-compiled modules. Porting large C programs from UNIX, MSDOS, INTROL, or Microware OS/9-68000 C to McCoah C is almost always a challenge.

Global variables (in McCoah C) must be actually declared once and noted as "extern" in all other modules. The manner in which this is normally done is to construct a header file providing all extern variables in a common block. This header file is "#include'd in all modules. Then the variables are actually defined in one of the modules.

This procedure, for some reason, even when followed faithfully, does not always work properly. Error messages such as "entry name clash ..." or "... unresolved in ..." are sometimes generated incorrectly. Often, it is necessary to actually include the header file in each module to circumvent the linker problems. Version 27 of the McCosh C compiler has the same linkage problems as version 26 and older editions.

I do not now have the details of the changes in the new Microware OS/9-68000 C; however, I will provide them when I get them. I have learned that it is a major, not a maintenance, release, since even those with maintenance contracts must pay for it, and there are new manuals associated with it. Contact Microware for details.

CURSES ONE-SCREEN EDITOR

The power of the curses package, discussed in the last chapter, is illustrated in the C program listed below. It is a one-screen editor, using the curses functions, adapted from an AT&T-supplied set of examples for the use of curses. Although the example program is not useful in itself, the edit function in the program could be very useful in a program which manages a screen window representing a portion of a file being edited. Even if the curses package is not available on a particular machine, the edit function could be used as a model for the development of a screen-oriented editor.

/* one-screen curses editor adapted from AT&T example program */

#include <curse.h>

short int c, row = 0, col = 0;

main(argc, argv)

int argc;

char *argv[];

```
{
    short int i, l, n;
    FILE *fd;

    if (argc < 2)
    {
        fprintf(stderr, "Usage: editor infile\n");
        exit(1);
    }
    if ((fd = fopen(argv[1], "r")) == NULL)
    {
        fprintf(stderr, "Could not read %s\n", argv[1]);
        exit(2);
    }
    initc();
    cbreak();
    nonl();
    noecho();
    idlok(stdscr, TRUE);
    keypad(stdscr, TRUE);
    while ((c = getc(fd)) != EOF)
        addch(c);
    fclose(fd);
    move(0, 0);
    refresh();
    i = edit();
    endwin();
    if (i)
    {
        if ((fd = fopen(argv[1] + (argc > 2), "w")) == NULL)
        {
            fprintf(stderr, "Could not write %s\n", argv[1]);
            exit(3);
        }
        for (l = 0; l < LINES - 1; ++l)
```

```
{
    for (n = len(l), i = 0; i < n; ++i)
        putc(winch(l, i), fd);
    putc('\n', fd);
    fclose(fd);
    exit(0);
}

len(lineno)
short int lineno;
{
    short int length;

    for (length = COLS - 1; ((length >= 0) && (winch(lineno, length) != ' ')); --length);
    return (length + 1);
}

edit()
{
    while (1)
    {
        move(row, col);
        refresh();
        switch (c = getch())
        {
            case KEY_LEFT: /* cursor left */
            case 'j':
                if (col)
                    --col;
                break;
            case KEY_RIGHT: /* cursor right */
            case 'l':
                if (col < COLS - 1)
                    ++col;
                break;
            case KEY_UP: /* cursor up */
            case 'k':
                if (row)
                    --row;
                break;
            case KEY_DOWN: /* cursor down */
            case ',':
                if (row < LINES - 1)
                    ++row;
                break;
            case KEY_HOME: /* cursor home */
            case 'h':
                move(row = 0, col = 0);
                refresh();
                break;
            case KEY_IL: /* insert line */
            case 'o':
                if (row >= LINES - 1)
                {
                    beep();
                    break;
                }
                move(++row, col = 0);
                insertln();
                break;
            case KEY_IC: /* insert characters */
            case 'c':
                standout();
                mvaddstr(LINES - 1, COLS - 20, "INSERT MODE");
                standend();
                move(row, col);
                refresh();
                while ((col < COLS - 1) && ((c = getch()) != 0x04) && (c != KEY_EIC))
                {
                    inach(c);
                    move(row, ++col);
                    refresh();
                }
            }
        }
    }
}
```



```

    }
    move(LINES - 1, COLS - 20);
    clrtoeol();
    refresh();
    break;
case KEY_DC: /* delete character */
case 'x':
    delch();
    break;
case KEY_DL: /* delete line */
case 'd':
    deleteln();
    break;
case KEY_CLEAR: /* redraw screen */
case 'z':
    clearok(curecr);
    refresh();
    break;
case 'w': /* write and quit */
    return 1;
    break;
case 'q': /* quit */
    return 0;
    break;
default:
    beep();
}
}

```

C BULLETIN BOARD

A bulletin board has been established by members of the Atlanta Computer Society Motorola Special Interest Group. It contains, among other areas, a public-domain C library and an amateur radio section. It currently operates at 300, 1200, and 2400 Baud. On your first call, you must register with the system operator (sysop) to be able to upload and download files. Be sure to mention that you learned of the bulletin board in C Notes. The telephone number is 404-493-4708.

C PROBLEM

The answer to the previous C problem, which was to code functions for multiplication, division, addition, and subtraction, implementing a generalized form of extended precision arithmetic, is provided as a part of the example C program below.

For the next problem, find the serious, but subtle, bug in the b-tree example program published several chapters back (six, to be more precise). [Hint: where does "gets(q)" place the string?] Provide two ways in which to fix the problem, and the advantages and disadvantages of each solution. There was also a typographical error in the original published listing, which caused a problem of its own, in function "caloc". The statement "x = ebrk(1 - n - a)" should read "x = ebrk(1 - n * a)".

EXAMPLE C PROGRAM

Following is this month's example C program; it implements an extended-precision reverse-polish calculator.

```

/* calculat.c - extended-precision reverse-polish
calculator */

#include <stdio.h>
#include <ctype.h>

#define MAXPREC 128 /* data length */
#define MAXSLOT 10000 /* max value (+ 1) per slot
(ends with zeroes) */
#define MAXSLOT2 16384 /* next larger power of 2 */
#define MAXDIGIT 4 /* digits per slot */

```

A bulletin board has been established by members of the Atlanta Computer Society Motorola Special Interest Group.

```

#define TYPE short int /* data type for numeric
and MAXSLOT * 2 */
#define DATA short int /* data type for MAXSLOT * 2
*/
#define LONG long /* data type for MAXSLOT *
MAXSLOT + 1 */

```

```

/* structure of each extended precision number:
*/
/* pmax maximum number of units of precision
*/
/* curr current number of units of precision
*/
/* (negative for negative number)
*/
/* data representation of extended number
*/
struct xprec
{
    TYPE pmax, curr;
    DATA data[MAXPREC + 1];
};

```

```

main(argc, argv)
int argc;
char **argv;
{
    char string[128];
    short int tos = -1, i;
    struct xprec rreg[17], *xreg[17];

    for (i = 0; i < 17; ++i)
        pzero(xreg[i] = &rreg[i]);

    while (fgetc(string, 128, stdin))
    {
        switch (*string)
        {
            case 'U':
            case 'I':
            case '2':
            case '3':
            case '4':
            case '5':
            case '6':
            case '7':
            case '8':
            case '9':

                digits:
                    pinput(string, xreg[++tos]);
                    poutput(string, xreg[tos]);
                    printf("%02d %e\n", tos,
                        xreg[tos]);

                    break;
            case '*':
                if (tos > 0)
                {
                    multiply(xreg[tos -
                        1], xreg[tos],
                        xreg[tos +
                        1]);
                    pcopy(xreg[tos + 1],
                        xreg[tos - 1]);
                }
            }
        }
    }
}

```



```

xreg[--tos]);
tos, string);
    }
    break;
case '/':
    if (tos > 0)
    {
        divide(xreg[tos -
                xreg[tos +
                1]);
        pcopy(xreg[tos + 1],
              poutput(string,
                    printf("X02d %e\n",
                          xreg[tos],
                          xreg[tos + 1]));
        xreg[tos - 1]);
        xreg[--tos]);
        tos, string);
    }
    break;
case '+':
    if (*(estring + 1) > 0x20)
        goto digits;
    if (tos > 0)
    {
        add(xreg[tos - 1],
            xreg[tos +
            1]);
        pcopy(xreg[tos + 1],
              poutput(string,
                    printf("X02d %e\n",
                          xreg[tos],
                          xreg[tos + 1]));
        xreg[tos - 1]);
        xreg[--tos]);
        tos, string);
    }
    break;
case '-':
    if (*(estring + 1) > 0x20)
        goto digits;
    if (tos > 0)
    {
        subtract(xreg[tos -
                xreg[tos +
                1]);
        pcopy(xreg[tos + 1],
              poutput(string,
                    printf("X02d %e\n",
                          xreg[tos],
                          xreg[tos + 1]));
        xreg[tos - 1]);
        xreg[--tos]);
        tos, string);
    }
    break;
case '=':
    if (tos > 0)
    {
        xreg[tos - 1] -> curr
        =
        compare(xreg[tos - 1], xreg[tos], 1);
        xreg[--tos] -
        > data[0] = 1;
        xreg[tos]);
        tos, string);
    }
    break;
case '~':
    if (tos > 0)
    {
        pcopy(xreg[tos],
              pcopy(xreg[tos - 1],
                    pcopy(xreg[tos + 1],
                          poutput(string,
                                xreg[tos + 1]);
                                xreg[tos]);
                                xreg[tos - 1]);
                                tos, string);

```

```

xreg[tos]);
tos, string);
    }
    break;
case '~':
    exit(0);
}
exit(0);
/* multiply(operand1 TIMES operand2 GIVES result)
*/
/* result may not be the same as operand1 or
operand2 */
multiply(operand1, operand2, result)
struct xprec *operand1, *operand2, *result;
{
    TYPE c1, c2, d, i, j, o1, o2, sign = 1;
    LONG c, l;
    struct xprec *op1 = operand1, *op2 =
    operand2;
    if ((result == op1) || (result == op2) ||
    pzero(result))
        return 2;
    for (c1 = abs(o1 = op1->curr);
        ((c1 > 0) && (!op1->data[c1 - 1]));
        --c1, (o1 > 0) ? --o1 : ++o1);
    for (c2 = abs(o2 = op2->curr);
        ((c2 > 0) && (!op2->data[c2 - 1]));
        --c2, (o2 > 0) ? --o2 : ++o2);
    if ((!c1) || (!c2))
        return 0;
    if ((c1 + c2) > result->pmax)
        return 1;
    if ((o1 > 0) != (o2 > 0))
        sign = -1;
    for (i = d = c = 0; i < c1; ++i)
    {
        for (j = 0, d = i; (j < c2) || c;
            ++j)
        {
            if (d >= result->pmax)
                return 1;
            l = (LONG)(result->data[d]);
            (((l >= c1) || (j >=
            c2)) ? c : (c +
            (LONG)(op1->data[i]
            * op2->data[j])));
            c = 1 / (LONG)(MAXSLOT);
            result->data[d++] =
            (TYPE)(l - (c *
            (LONG)(MAXSLOT)));
        }
        while ((d > 0) && (!result->data[d - 1]))
            --d;
        result->curr = d * sign;
        return 0;
    }
    /* divide(operand1 OVER operand2 GIVES result)
    */
    /* result may not be the same as operand1 or
    operand2 */
    divide(operand1, operand2, result)
    struct xprec *operand1, *operand2, *result;
    {
        TYPE c1, c2, d, i, j, k, m, n, o1, o2, p, q,
        sign = 1;
        struct xprec *op1 = operand1, *op2 =
        operand2;
        struct xprec dtemp, *pdtemp = &dtemp;
        struct xprec rtemp, *prtemp = &rtemp;
        struct xprec wtemp, *pwtemp = &wtemp;
        struct xprec xtemp, *pxtemp = &xtemp;

```



```

        struct xprec ytemp, *pytemp = &ytemp;
        struct xprec ztemp, *pztemp = &ztemp;

        if ((result == op1) || (result == op2) ||
            pzero(result) || pzero(pdtemp) || pzero(prtemp) ||
            pzero(pwtemp) || pzero(pxtemp) || pcopy(op1, pytemp)
            || pzero(pztemp))
            return 2;
        for (cl = abs(ol = op1->curr);
             ((cl > 0) && (lopl->data[cl - 1]));

            --d;
            result->curr = d * sign;
            return 0;
    }

    /* divide(operand1 OVER operand2 GIVES result)
    */
    /* result may not be the same as operand1 or
    operand2 */
    divide(operand1, operand2, result)
    struct xprec *operand1, *operand2, *result;
    {
        TYPE cl, c2, d, i, j, k, m, n, ol, o2, p, q,
        sign = 1;
        struct xprec *op1 = operand1, *op2 =
        operand2;
        struct xprec dtemp, *pdtemp = &dtemp;
        struct xprec rtemp, *prtemp = &rtemp;
        struct xprec wtemp, *pwtemp = &wtemp;
        struct xprec xtemp, *pxtemp = &xtemp;
        struct xprec ytemp, *pytemp = &ytemp;
        struct xprec ztemp, *pztemp = &ztemp;

        if ((result == op1) || (result == op2) ||
            pzero(result) || pzero(pdtemp) || pzero(prtemp) ||
            pzero(pwtemp) || pzero(pxtemp) || pcopy(op1, pytemp)
            || pzero(pztemp))
            return 2;
        for (cl = abs(ol = op1->curr);
             ((cl > 0) && (lopl->data[cl - 1]));
             --cl, ((ol > 0) ? --ol : ++ol));
        for (c2 = abs(o2 = op2->curr);
             ((c2 > 0) && (lo2->data[c2 - 1]));
             --c2, ((o2 > 0) ? --o2 : ++o2));
        if ((lc1) || (c2 > cl) || (compare(op1, op2,
        0) < 0))
            return 0;
        if (lc2)
            return 1;
        if ((ol > 0) != (o2 > 0))
            sign = -1;
        for (d = cl - c2; d >= 0; --d)
        {
            for (n = 0, m = d; m < cl; )
                pwtemp->data[n++] = pytemp->data[m++];
            pwtemp->curr = n;
            if ((k = compare(pwtemp, op2)) <= 0)
            {
                if ((result->data[d] = (k +
                for (m = d; m < cl;
                    pytemp->data[m] = 0;
                continue;
            }
            for (i = MAXSLO2, j = q = 0; i; )
            {
                pxtemp->curr = -1;
                pxtemp->data[0] = k = j +

```

```

        (i >>= 1);
        pdtemp)) &&
        prtemp)) &&
        pztemp);
        if ((multiply(op2, pxtemp,
            pdtemp, pwtemp,
            prtemp->curr >= 0))
            {
                q = j = k;
                pcopy(prtemp,
                    if (lprtemp->curr
                        break;
                )
            }
        if (q)
            for (result->data[d] = q, n
                = 0, m = d; m < cl; )
                pytemp->data[m++] =
                pztemp->data[n++];
            for (d = cl - c2 + 1; ((d > 0) && (lresult-
                >data[d - 1])); --d);
            result->curr = d * sign;
            return 0;
        }

        /* add(operand1 PLUS operand2 GIVES result)
        */
        /* result may not be the same as operand1 or
        operand2 */
        add(operand1, operand2, result)
        struct xprec *operand1, *operand2, *result;
        {
            TYPE cl, c2, d, ol, o2, e1 = 1, e2 = 1, sign
            = 1;
            LONG e, l;
            struct xprec *op1 = operand1, *op2 =
            operand2;

            if ((result == op1) || (result == op2) ||
                pzero(result))
                return 2;
            for (cl = abs(ol = op1->curr);
                 ((cl > 0) && (lopl->data[cl - 1]));
                 --cl, ((ol > 0) ? --ol : ++ol));
            for (c2 = abs(o2 = op2->curr);
                 ((c2 > 0) && (lo2->data[c2 - 1]));
                 --c2, ((o2 > 0) ? --o2 : ++o2));
            if (lc1)
                return (pcopy(op2, result));
            if (lc2)
                return (pcopy(op1, result));
            if ((ol < 0) || (o2 < 0))
            {
                if ((ol < 0) && (o2 < 0))
                    sign = -1;
                else
                {
                    switch (compare(op1, op2,
                    0))
                    {
                        case -1:
                            e1 = -1;
                            if (o2 < 0)
                                sign = -1;
                            break;
                        case 0:
                            return 0;
                        case 1:
                            e2 = -1;
                            if (ol < 0)
                                sign = -1;
                            break;
                    }
                }
            }
            for (c = d = 0; (d < cl) || (d < c2); )
            {
                l = c + (LONG)((d < cl) ? (e1 * op1->
                >data[d] : 0) +
                ((d < c2) ? (e2 * op2->
                >data[d] : 0));

```



```

        c = 1 / (LONG)(MAXSLOT);
        if ((1 - (c * (LONG)(MAXSLOT))) < 0)
            1 += (LONG)(MAXSLOT), --c;
        if (d >= result->pmax)
            return 1;
        result->data[d++] = (TYPE)(1);
    }
    if (c > 0)
    {
        if (d >= result->pmax)
            return 1;
        result->data[d++] = (TYPE)(c);
    }
    while ((d > 0) && (!result->data[d - 1]))
        --d;
    result->curr = d * sign;
    return 0;
}

/* subtract(operand1 MINUS operand2 GIVES result)
*/
/* result may not be the same as operand1 or
operand2 */
subtract(operand1, operand2, result)
struct xprec *operand1, *operand2, *result;
{
    struct xprec atemp, *ptemp = &atemp;

    if (negate(operand2, ptemp))
        return 2;
    return (add(operand1, ptemp, result));
}

/* compare(operand1 TO operand2 WITH signa)
*/
/* value is -1, 0, +1 if operand1 <, =, > operand2
*/
/* operand1 and operand2 unsigned if signa = 0
*/
compars(operand1, operand2, signa)
struct xprec *operand1, *operand2;
short int signa;
{
    TYPE c1, c2, d, o1, o2, a1 = 1, s2 = 1;
    struct xprec *op1 = operand1, *op2 =
operand2;

    for (c1 = aba(o1 = (signa ? op1->curr :
aba(op1->curr)));
        ((c1 > 0) && (!op1->data[c1 - 1]));
        --c1, ((o1 > 0) ? --o1 : ++o1));
    for (c2 = aba(o2 = (signa ? op2->curr :
abs(op2->curr)));
        ((c2 > 0) && (!op2->data[c2 - 1]));
        --c2, ((o2 > 0) ? --o2 : ++o2));
    if (o1 < o2)
        return (-1);
    if (o1 > o2)
        return 1;
    if (o1 < 0)
        a1 = -1;
    if (o2 < 0)
        s2 = -1;
    while (--c1 >= 0)
        if (d = ((op2->data[c1] * s2) - (op1-
>data[c1] * a1)))
            return ((d < 0) ? 1 : -1);
    return 0;
}

/* pcopy(operand INTO result)
*/
pcopy(operand, result)
struct xprec *operand, *result;
{
    memcpy(result, operand, sizeof(struct
xprec));
    return 0;
}

```

```

/* negate(operand INTO result)
*/
negate(operand, result)
struct xprec *operand, *result;
{
    if (pcopy(operand, result))
        return 2;
    result->curr *= -1;
    return 0;
}

/* pzero(operand)
*/
pzero(operand)
struct xprec *operand;
{
    int i;

    operand->pmax = MAXPREC;
    for (i = operand->curr = 0; i < MAXPREC; ++i)
        operand->data[i] = 0;
    return 0;
}

/* pinput(string INTO operand)
*/
pinput(string, operand)
char *string;
struct xprec *operand;
{
    char *p = string;
    TYPE temp, sign = 1, ptn;

    if (*p == '-')
        sign = -1;
    for (operand->curr = temp = 0, p +=
(strlen(p) - 1), ptn = 1;
        p >= string; --p)
    {
        if (ptn >= MAXSLOT)
        {
            if (operand->curr >=
operand->pmax)
            {
                operand->curr *=
sign;
                return 1;
            }
            operand->data[operand->
curr++] = temp;
            temp = 0;
            ptn = 1;
        }
        if (isdigit(*p))
        {
            temp += (*p - '0') * ptn;
            ptn *= 10;
        }
    }
    if (temp)
    {
        if (operand->curr >= operand->pmax)
        {
            operand->curr *= sign;
            return 1;
        }
        operand->data[operand->curr++] =
temp;
    }
    operand->curr *= sign;
    return 0;
}

/* poutput(estring FROM operand)
*/
poutput(string, operand)
char *string;
struct xprec *operand;
{

```



```

char *p = string, form[10];
TYPE slot = operand->curr;

if (slot < 0)
{
    slot += -1;
    strcpy(p++, "-");
}
while ((--slot >= 0) && (looperand-
>data[slot]));

```

```

aprintf(p, "%d", (slot < 0) ? 0 : operand-
>data[slot]);
aprintf(form, "%c%c%d%c", 'Z', '0', MAXDIGIT,
'd');
for (--slot, p += strlen(p); slot >= 0; --
slot, p += MAXDIGIT)
    aprintf(p, form, operand-
>data[slot]);
return 0;
}

```



SARDIS

**512K RAM
Expansion**

TECHNOLOGIES

Last year we reviewed several SBCs. One of which was the Sardis ST-2900 6809 SBC. If you remember I installed it into a Heath H19 CRT terminal, with two 5 inch drives. The system drive 80 track, the work drive a 40 track drive. It makes a very nice package. The two major problems with this system was 1.) a level one system and 2.) memory problems. However, most of that has been rectified with their latest line addition - a 512K RAM expansion, with RamDisk software.

The addition of the 512K expansion board was a real advantage. I spend most of my time programming in C and SCULPTOR+. While Sculptor+ is not at it's best on a level one system, it suffices for most of my projects. Actually I discovered that over 70% of all my Sculptor projects can be done on a level one system. As for C, well, I do most all my 6809 programming on the level one Sardis system in C. The Sardis system uses the Tandy R/S version of OS-9 and some special drivers from Sardis/D.P. Johnson. By using this version I found that the CoCo OS-9 leaves more available RAM than any other level one system I know of. So the 512K expansion has made life with level one a lot sweeter. For FLEX it is also very efficient and some of the enhanced utilities furnished make file handling very fast.

We have several different 6809 FLEX, OS-9 and UniFLEX systems with expanded RAM, up to a full meg on several, however, the Sardis 512K expansion is the least expensive of them all. And took less than a half hour to install.

The actual installation time was spent in prying apart the PDC (floppy disk controller) from the CPU board and inserting the 512K expansion board. The package is now a three board sandwich. Also we opted to install our own memory chips (256k). The price for these has fallen considerably in recent weeks. The full set of chips cost us about \$45.00. And since the rest of the board had been factory built and tested everything went very smooth. The instructions were complete and easy to understand. A usual Sardis touch.

The 512K expansion uses a fully transparent refresh scheme. The CPU accesses memory at full speed (no wait states). Also an efficient checksum routine insures the integrity of RamDisk data. This should preclude total system crashes by checking each sector as it is read or written and reporting the error immediately. Partial data corruption by line glitches, etc. will be less likely to bomb your entire work session. And of course you should run the VERIFYND (see below) at least once a day (providing your system is never turned off) to insure nothing has clobbered part of the RamDisk.

The documentation is very complete. Full circuit diagrams, parts list and parts placement charts, PAL logic diagrams (factory and board level), technical notes and a special RamDisk memory test utility.

The RamDisk is defined to contain 16 256 byte sectors. Each fits exactly into one 4K page on the 512K board. Therefore, the board contains 128 such pages. Page 0 is used to replace the \$E0000-\$EFFF memory on the CPU board. Page one is reserved for storing the checksum table, leaving 126 track for a total of 2016 available sectors. FLEX automatically extends the directory as needed. Because of the high speed of a RamDisk, fragmented directories and files are of little concern.

Each sector has a two byte checksum, and since there are 2016 sectors, all the checksums fit exactly into one 4K page. The RamDisk speed is such that the checking of checksums is not noticeable and creates confidence and peace of mind in regards to data integrity. The RamDisk and the special features from Sardis make FLEX a much more efficient system.

The FLEX system (the Sardis SBC supports both FLEX and OS-9, just insert the proper disk and boot) becomes much more efficient running in RamDisk. I use the special copy command from Sardis (much faster) and load most used commands and work files into the 512K RamDisk. You cannot imagine the difference in efficiency. About every 10 minutes I backup to the work disk the current project in RamDisk (your zoned in if the power flicks) and have not yet lost a single bit. I estimate that things go 5 to 6 times faster in RamDisk than on a physical disk. Just remember to make timely backups!

RAMDSK29 is the program that activates the RamDisk device drivers. It has several options. A "N" implies do not reformat the RamDisk and don't test for checksum errors. A "Y" implies yes, do reformat the RamDisk but do not test for checksum errors. A "E" implies to reformat the disk only if checksum errors are detected. RAMDSK29 should be in the startup file, and run each time the system is brought on line. Additional options are:

TK=ddd number of tracks to allocate.

DR=d drive number to assign (default 3).

The RAMDSK29 also patches FLEX to greatly speed up the "LOADCODE" system code. If the RamDisk data is still intact reformatting of the RamDisk may not be necessary. RAMDSK29 is used by FLEX only.

VERIFYND command (FLEX & OS-9) is used to test every sector of the RamDisk for checksum errors. Options are the same as RAMDSK29. Time to completely check all 126 tracks is approximately 8 seconds.

FCOPY (FLEX only) is much faster than the regular FLEX copy routine and makes loading the RamDisk much faster. A ratio of 2 to 7 is typical. The main limitation is that FCOPY can only copy one file per call. Options are:

D implies that FCOPY should use the current system date. If omitted the date remain the same as that of the input file.

S tells FCOPY to use a 1K buffer in order that it will fit in the UCA (\$C100-\$C6FF). Otherwise FCOPY will use all of user RAM as a buffer. This is necessary from programs such as calls from TSC's BASIC.

MENTEST test all 512K bytes and uses routines from the Sardis monitor ST-Mon. By using the monitor "D F" command sequence it can run on an OS-9 system also. Test patterns and error message are displayed on the system CRT.

For the OS-9 system the disk is formatted by the regular Sardis SFORMAT. A driver RAMDSK09 and a descriptor file RU are used in normal fashion by loading. The RamDisk is defined "RU".

The net result is that the Sardis 512K expansion is a worthy addition. Once you get into the swing of having the extra ram, it becomes essential.

For additional information or to order your 512K expansion, see Sardis Technology advertising, this issue.

OS-9

User Notes

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Standards

Standards are IMPORTANT, that's why I'm coming back to them again. Last time I wrote about standards I had directory structures in mind; the time before that it was terminal support. In a way I'm hitting the terminal support issue again.

Consider the Atari ST -- I think it is almost inevitable that OS-9 will be available for it soon. Consider the Commodore Amiga -- I'm not so sure about it, but I'd be surprised if you don't see OS-9 there too. Excellent! Two more large groups of OS-9 users will make a big difference. We'll see lots of new software. We'll be able to buy powerful, expandable, inexpensive computers. Our favorite operating system will be a little more widely known.

Now consider the ST again. It's got a music chip, fancy video hardware and some special keys. Customers for OS-9 on the ST will very reasonably demand support for those features. Amiga owners have machines that are even more special. The music is stereo and video hardware includes elaborate support for moving graphics. If the ST or Amiga crowd discovers OS-9 and adds hundreds of thousands of new OS-9 users to our group what will that do for us? Not much. It might even hurt.

A software company will seldom write programs for the lowest common denominator (they would never compete). They'll target a large group of likely customers and try to create something that they'll find irresistible. That means that the large group of CoCo users (and perhaps the groups of ST and Amiga users) will see lots of OS-9 software that exercises all their machines' abilities. Folks with oddball systems and ANSI terminals like me will only be able to run a little of the stuff.

We've already seen a little of this with the CoCo. Compared to the new 68000-based machines the CoCo is pretty dull, but even so there is plenty of CoCo-specific OS-9 software.

A few years ago every OS-9 user had an oddball system with his own favorite terminal. Software developers had to find clever ways to write programs that could adapt or be adapted. It wasn't easy to do, and the programs never worked quite as well as they would have if they were custom-written for specific hardware. For example, no editor on OS-9 uses more than a small fraction of my terminal's features. Back when we were an anarchistic bunch there wasn't much software available, but what there was would run on my system (or it was defective).

The Unix community is more diverse than we were, but much of their software adapts nicely to its environment. I use Unix on three very different types of computer. I use at least five types of terminal. In general, everything but the programs that use graphics work for any combination. Even some graphics programs can work through various permutations. Of course, the programs are large and make heavy use of nice standards (like termcap files).

So maybe I should get on my soap box and call frantically for standards. The idea is tempting, but foolish. It would be wasted energy. Hardware manufacturers will look for special features to distinguish their machines from others. If enough people buy the computer to make it a success by today's

standards, software companies will write programs to use all its features -- including the unique ones. So much for standards.

There are some glimmers of hope. If you get a computer that supports graphics at the approximate level of the Hitachi chip much of the graphics software written for OS-9 systems may work on your system. This is particularly likely if at least two comparable machines make a big splash. Software vendors may feel moved to use the graphics standard, VUI, which Microware has adopted if it lets them sell a single program into two (or more) big markets.

The same effect may work for simple full-screen programs. Microware has defined a de facto standard for terminal description called the termcap file. Perhaps it will be used for programs that don't need particularly good screen control.

The structure of OS-9 almost enforces certain standards. We are unlikely to be caught in the deadfalls that keep dropping on PC-compatible owners. OS-9 doesn't have entry points -- much less undocumented entry points. Doing physical I/O from within an OS-9 program is uncomfortable and unlikely. Device drivers and file managers can be written by anyone and used by anyone with suitable hardware. Microware has given us standards for SCF, RBF, and SBF devices. There are new standards for networks and graphics. With luck these standards will be widely supported. Even with poor luck there is a good chance that programmers will stick with OS-9's layered structure. Accessing a non-standard piece of hardware through a file manager and device driver is almost as good as strict adherence to standards.

Now I'll mount my soap box. If you decide to write software for the upcoming sexy OS-9 machines, take advantage of all the features you can, but do it within the layered structure of OS-9. First an appeal to your pride: I'm talking about good software engineering practice. Modularity and abstraction rate right up with mom, apple pie, and a work station on every desk. Second an appeal to your avarice: OS-9 is on its way up. A better machine and a bigger market are always just around the corner. If you design your software so hardware dependencies are isolated in device drivers and protocols are isolated in file managers you'll find it much easier to port your software to the next hot machine.

So hope for lots of competition in the OS-9 hardware market. Buy flexible computers if you possibly can. Stay away from non-standard features unless they are very popular or you can run without them. Beat of all stick with your current system a while longer. Great things are (always) just around the corner.

You may remember that I was planning to buy a 68K system months ago. I found the OS-9/68K operating system so much better than straight OS-9 that I was going to throw all my 6809 software to the winds and move. I haven't got a new system yet. I have to admit that part of the reason is being married. The important reason is, however, that I can't make up my mind.

There are several single-board OS-9/68K systems running from the Cimix down in price and performance. They are all nice packages and the prices are nice but none of them can easily accommodate memory management. Cimix may come out with a 68020 + memory management board but it isn't here yet. I can't bring myself to spend enough to get a OS-9/68K system on a throw-away machine, and I want more out of a computer than any of the current generation of systems offer. A

well-supported expansion bus would do a lot to make me more comfortable with a computer. I could buy one now and add to it as my budget and needs dictate, but a good system with a bus is fiercely expensive. I'm still perched on the fence.

The fence is a good place to be now. If some new computer comes along and grabs a big chunk of the OS-9 market, I can jump on the band wagon and be one of the people demanding special support instead of whimpering about standards. It's easier being on the winning side.

Great Things

I thought I would have definite news about the ST or Amiga by now. I've also been sitting on the edge of my seat about an even more important OS-9 happening. I can't wait any more. This column must go in now. If the "happening" happens soon I'll send a special "extra" column to Don, perhaps he'll be able to squeeze in a few more words at (or after) the last minute. Otherwise look forward to next month. Surely it will have happened by then! Your columnist is fairly bouncing with impatience.

An Introduction To The

G-64 Bus

By Cosma Pabouctwidia
GESPA, Inc.

In recent years, the Eurocard/DIN form factor for board level microcomputer products has become the favorite choice for an increasing number of industrial OEMs. The most publicized buses using this format, however, have until now been targeted toward the high performance end of the board spectrum. These buses are usually implemented on large and expensive boards, need complex bus arbitration overhead, and are often an "overkill" for most simpler 8 and 16-bit applications. The G-64 bus, already widely popular in Europe, was introduced in the U.S. in late 1984 by GESPA, Inc. (Mass, AZ). The G-64 bus fulfills the need for a compact, simple, inexpensive yet powerful, industrial grade family of microcomputer boards. With seven years of experience in the European industry, the G-64 is a proven design, backed by over 25 manufacturers offering more than 400 different G-64 modules and support software. Recent improvements to the original bus specification have been made to allow the G-64 bus to remain one of the best supports for most popular 8 and 16/32-bit microprocessors.

USING THE G-64 BUS

The G-64 bus is a second generation, processor independent, non-multiplexed 16-bit microcomputer bus aimed at low end and midrange industrial applications. The bus was first defined by GESPA in 1979 and second sourced by France's Thomson-CSF in 1980. The bus is an open architecture and no licensing is necessary in order to build compatible products. Since its introduction in 1979, the G-64 bus has become a favorite for control applications in various industries including: semiconductor capital equipment, food processing, textile, plastic injection, and medical equipments. The bus is also widely used in several factory automation, process control and robotics applications. Also, the G-64 bus is often found in automatic test equipment, either fixed, portable or airborne, and data acquisition and remote control/monitoring systems. Because of its size and cost advantages, a G-64 bus system often serves as a front-end microcomputer to a more powerful number cruncher based on more sophisticated bus structures in a networked system architecture.

G-64 BUS ARCHITECTURE

The G-64 bus board uses the standard single height Eurocard form factor of 100mm by 160mm (4" by 6.25") which is the smallest allowed in the Eurocard specification matrix shown in figure 1. The bus also uses the 96 pin DIN 41612 pin-in-socket connector. This connector offers higher pin density and improved performance over conventional card edge connectors. The rugged Eurocard/DIN connector design of the G-64 bus allows the cards to operate with a very high level of reliability in the most hostile environments. Electrically, the G-64 bus uses five types of lines: data, address, control, interrupt, and power supply. Figure 2 shows the pin assignment. The bus is processor independent and today the 8085, Z-80, 6809, 8088, 80286, 68000, 68010, 32016 and the PDP-11/70 compatible J-11 processors are all available on the bus. The bidirectional data bus uses 16 lines to handle all data transfer, whether to memory or peripheral. The direction of the data flow is determined by a single Read/Write signal. The G-64 bus specification allows for several levels of complexity and compliance. This architecture allows for the flexibility needed to build boards that range from the simplest, and therefore the least expensive, to the most powerful, while imposing a strict guideline of upward compatibility. Figure 3 shows this layered concept. The most elementary level is the G-64's I/O map, which is in fact a subset of the main system's bus. The I/O map of the G-64 bus requires only 10 address lines, validated by a peripheral access strobe signal VPA* to decode a 1K word peripheral address space. This in turn greatly simplifies the design of a typical G-64 bus I/O card, as shown in figure 4, which permits the most efficient use of the board's real estate. This simpler architectural concept is of particular benefit to the user who designs boards specific to his application.

FULL 16-BIT CAPABILITY

In the original G-64 specification, memory is accessed through the decoding of the 16 address lines and the page line, which when validated by the VMA* signal, provides direct access to up to 256 Kilobytes on the standard bus. This addressing capability is all that is necessary for the implementation of 8-bit and simple 16-bit microprocessors. In order to properly support the most recent 16-bit microprocessors, the bus was revised in 1984 and expanded to use a 96 pin connector which provides 32 additional lines to the original

specification. These lines on the expanded G-64 bus, or G-96 bus, allow the addressing capability of the bus to be expanded to 32 Megabytes, and provide the necessary signals for the implementation of a powerful multiprocessing arbitration scheme, while guaranteeing backward compatibility with the simpler G-64 boards. At all levels of sophistication, the G-64 bus provides support for six interrupt levels; five interrupt request lines (IRQ1* to IRQ5*) and one non maskable interrupt line (NMI*). The G-64 bus supports vectored and non-vectored (auto-vectored) interrupts. For vectored interrupts, the interrupting device initiates the interrupt sequence by activating the interrupt request line of the bus. When the CPU accepts the interrupt and begins servicing it, it sends out an interrupt acknowledge (IACK*) signal. When the interrupt-requesting module receives the IACK* signal, it places its interrupt vector on the data bus. The CPU uses this vector in order to quickly jump to the proper interrupt service routine. Non-vectored, or auto-vectored interrupts are needed to support the simplest and least expensive I/O modules, those modules not equipped with vector generation capability. In this case the interrupted CPU will jump to a predetermined program location. If more than one module requests the bus for interrupt at the same level, daisy-chain-in and daisy-chain-out lines assign a priority to each request based on the requesting module's position on the bus; the module closest to the CPU is given first access. Figure 5 illustrates the daisy chain's use. Other important lines of the bus are the RESET* line, and the power fail detect line PWF*. The reset line is pulled down to a low level at power-up to initialize the CPU and other parametizable modules on the bus. The power fail line is used to indicate to the CPU an imminent loss of power and to save the most valuable working parameters. The G-64 bus also supports Direct Memory Access from several sources. This DMA capability allows devices with high data throughput, such as disk and local area network controllers, to efficiently use the bus. In a typical sequence, the DMA requesting device initiates a sequence by pulling the Bus Request line low (BRQ*). The CPU grants the bus by asserting the bus grant (BGRT*) signal. Finally, the requesting device acknowledges its control of the bus by asserting the bus grant acknowledge line active (BGACK*), and keeps this line low for as long as the bus is in its control. The same daisy chain interrupt priority scheme is used for the Direct Memory Access functions. The G-64 bus carries three voltages: +5V, +12V and -12V. Most G-64 modules operate out of the +5V power supply. The +12V and -12V are primarily used to provide power to RS-232 drivers and analog converter modules. Also, the bus provides a +5V standby line to connect a battery for powering such devices as CMOS RAM or a clock/calendar.

DYNAMIC CHARACTERISTICS OF THE BUS

Timing-control and clock lines on the bus help regulate the data flow and provide timing signals to peripheral devices and memories. Depending on the microprocessor supported, the G-64 bus can operate in either synchronous or asynchronous data transfer mode. In the synchronous mode, all bus transfer occur synchronously to a master clock frequency, usually equal to a normal microprocessor instruction cycle. The G-64 bus specifies synchronous transfer rates up to 4 Megabytes per second. The asynchronous mode is supported mostly by the 8-bit microprocessors, and related memory and I/O devices. In the asynchronous mode, data transfer is totally independent of any system clock. In this mode the CPU usually initiates a transfer with a memory device and the memory in turn informs the CPU that the transfer has been successfully completed using two handshaking signals. This transfer mode allows the CPU to operate at the fastest possible speed allowed by the memory or peripheral device that is accessed. The G-64 bus will operate in asynchronous mode whenever 16-bit microprocessors are used, and the maximum speed in this mode approaches 10 Megabytes per second. Two pins on the bus will have a slightly different function depending on the transfer mode. The Valid Memory Access line (VMA*) which is used in the asynchronous mode to indicate that a valid address of the memory map is available on the bus, initiates the beginning of the memory cycle in the

asynchronous mode. The READY line which is used in the asynchronous mode to stretch the memory cycle to accommodate slower memory devices, is used as the Data Transfer Acknowledge (DTACK*) line signaling the completion of a data transfer in the asynchronous mode. The transfer mode used mainly effects the access to memory devices; an asynchronous 16-bit CPU will require an asynchronous 16-bit memory, while a 8-bit CPU will require a synchronous 8-bit memory. Typically, peripheral devices are to be accessed in a synchronous manner, with asynchronous mode as a jumper option. The asynchronous I/O mode allows full advantage to be taken of the fast peripheral devices now available in the industry.

MULTIPROCESSING ON THE G-64 BUS

In the quest for increased system performance and speed, a recent trend is to have several microprocessors handle the task that was previously handled by one, all of them operating simultaneously on the same bus. A typical example of such an application would be the control of a robot's arm where one microprocessor would be assigned to supervise each of the arm's axis, using the common bus to communicate at very high speeds with one another. Two types of multiprocessing architecture are supported on the G-64 bus. The first relies on a Master/Slave approach, where one microprocessor card (master) supervises several other microprocessors (slaves) dedicated to an I/O function. In such an architecture, the master communicates with each slave through a dual ported memory located on the slave processor. This multiprocessing architecture has the dual advantage of being simple to implement and simple to program. Since the tasks are clearly defined for each processor on the bus, the amount of data exchanged on the same bus is concise and minimal. The most recent addition to the G-64 bus specification allows a decentralized, parallel multibus configuration, whose implementation is optional. The actual implementation of the multiprocessing capability requires six lines for the priority identifier (P0*-P5*), a bus busy signal (BBUSY*) and an arbitration clock (ARBCLK). When a module wishes to take control of the bus, it places its unique 5 bit identifier code on the priority identifier lines. If another module initiates an arbitration at the same time, its code gets wire-or'd on the bus. A priority resolution network resident on each CPU module, then examines the P0*-P5* lines. If the identifier found on these lines is the same as the module's, it then wins the bus. Otherwise, control of the bus goes to another module with higher priority. Figure 6 shows the logic necessary for the implementation of this powerful multiprocessing scheme. The bus priority logic is duplicated and resides on every one of the processor boards of the system. This feature eliminates the need for a central bus controller which would paralyze the entire system in case of failure. The priority level of a given processor board can be programmed dynamically by software and is therefore independent of the geographic position of the board in the backplane. The main advantage of this architecture is to offer a permanent arbitration, in such a way that a current bus master is immediately informed when there is a higher priority module requesting the bus. If the current bus master's priority is lower than the requester, the master could still keep the bus. However, by monitoring the arbitration, it would release the bus since it has lost the arbitration. The arbitration principle allows implementation of up to 32 priority levels with "protest" feature which allows the bus requester to obtain temporarily the highest priority level. Another feature of the G-64 bus arbitration is the arbitration with "fairness", in which a module releasing the bus will not participate in the arbitration before all requesters have been serviced. In a multiprocessor system it is necessary to determine which processor is to respond to a given interrupt. In addition, it is not possible to maintain an interrupt request asserted since this would lock the bus while the interrupt is being processed. To resolve these issues, the G-64 bus supports an event peering structure. An event is a short message of two words or more which contains primarily the ID of the requesting device and the ID of the CPU involved. Event messages transfers are performed on the data bus and synchronized by the Valid Event Data (VED*) signal.

CONCLUSION

The unique features of the G-64 bus make it very attractive to an important category of system integrators. Its simple and flexible structure already accommodates most current microprocessor technologies:

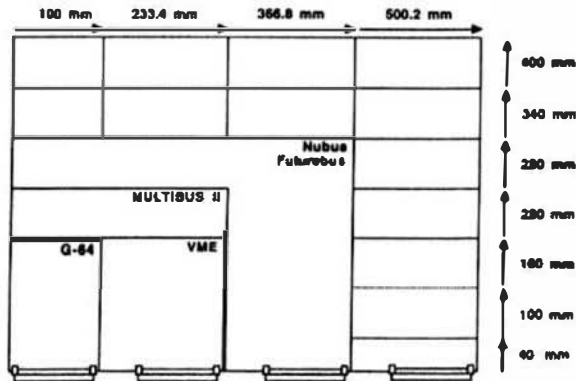


Figure 1: The G-64 bus is the only 8/16-bit bus exclusively defined for the single height Eurocard form factor.

	ROW C	ROW B	ROW A		Definition
1	GND	GND	GND	1	Power
2	A16	A8	A0	2	Address lines A0 to A23
3	A17	A9	A1	3	
4	A18	A10	A2	4	
5	A19	A11	A3	5	
6	A20	A12	A4	6	
7	A21	A13	A5	7	
8	A22	A14	A6	8	
9	A23	A15	A7	9	
10	Reserved	BRQ	BCHT	10	Control & Interrupt lines
11	Reserved	DS1	DS0	11	
12	Reserved	BGACK/BBUSY	HALT	12	
13	GND	Enable	SYCLK	13	
14	Reserved	Reset	VPA	14	
15	Reserved	NMI	RDY/DYACK	15	
16	IRQ3	IRQ1	VMA	16	
17	IRQ5	IRQ2	R/W	17	
18	VED	IACK	IRQ4	18	
19	GND	D12	D8	19	Data lines D0 to D15 & Arbitration lines
20	P5	D13	D9	20	
21	P4	D14	D10	21	
22	P3	D15	D11	22	
23	P2	D4	D0	23	
24	P1	D5	D1	24	
25	P0	D6	D2	25	
26	Reserved	D7	D3	26	
27	SYSFAIL	BERR	Page	27	Misc.
28	ARBLCK	Chain In	Chain Out	28	
29	Reserved	+ 5V bat.	PWF	29	Power
30	Reserved	- 12V	+ 12V	30	
31	+ 5V	+ 5V	+ 5V	31	
32	GND	GND	GND	32	

Figure 2: The bus supports 16-bit of data and most other features expected of a modern bus.

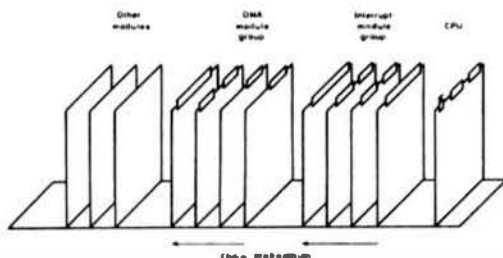


Figure 5: A delay-chain priority scheme is used to arbitrate interrupts and DMA requests.

all-CHOS boards are being introduced on the bus, and 32-bit microprocessors will soon be available. New developments are easily adapted to the bus architecture, ensuring the G-64 a position of growing importance in the bus line-up. NOTE: * indicates an active low signal.

SIMPLEST
↓
MOST POWERFUL



Figure 3: The G-64 bus specification allows for simple boards to be used in conjunction with the most powerful microprocessors.

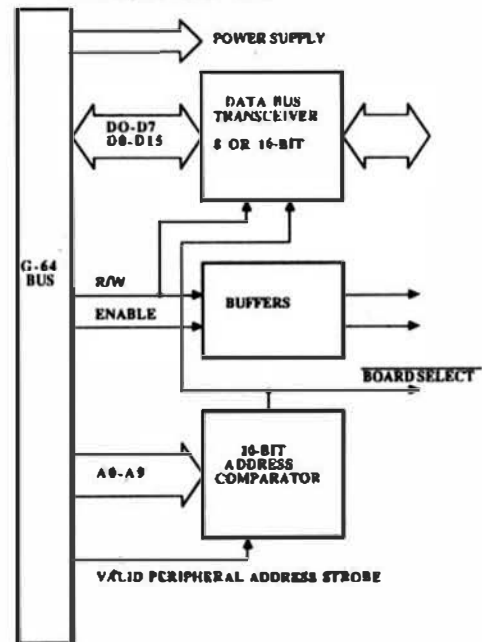


Figure 4: A typical I/O interface to the G-64 bus can be implemented in less than 5 TTL LS devices.

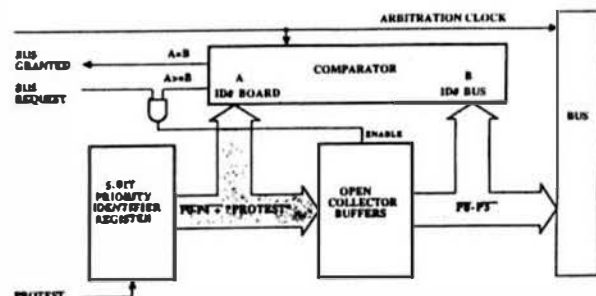


Figure 6: The G-64 bus allows for a sophisticated decentralized multi-processing arbitration scheme.



MOTOROLA

MC146805E3

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One of the first entries into the CMOS family of 8-bit computers was the MC146805E2. This microprocessor provided the user with not only two on-chip 8-bit I/O ports, 112 bytes of RAM, 8-bit Timer, multiplexed Address/Data bus, but a memory map of 8k bytes. This was more than sufficient in the beginnings of the "minimum chip count" systems, when CMOS EPROMS and masked ROMs were of relatively small memory size.

This MPU became the cornerstone of Motorola's CMOS architecture, with an efficient Instruction set, true Bit Manipulation, and 3 to 6 volt operation. When integration of all members of a system became viable in the CMOS process, the E2's structure was carried into the MC146805G2, MC146805F2, and EPROM versions of the same devices.

In the early beginnings of MCU code generation, it was thought that a memory map of 8k would be sufficient for most controller type of applications. It was also thought that more than 8k would not be necessary for most applications. Since the 'E2 was expandable, many applications started using only segments of the 8k address space. Later, EPROMS became more inexpensive, marketers promised more features, and software writers were pressed into code compaction scenarios on almost every project.

For many applications, a large address space full of ROM or EPROM may mean either inefficient code generation, or a product with features which may overwhelm the processing power of the host MCU. On the other hand, there are applications which have neither of the above afflictions.

Take for instance an application which uses over 16k of ROM, but still does not tax the capabilities of the 6805. A recently designed HF radio transceiver has features which include: Band Scan, Memory Scan, Real Time Clock, Teletype and CW decode, direct frequency entry, Optical Encoder tuning, and remote control via RS-232. Most of these functions are mutually exclusive, and have little interaction upon one another.

Initially, the project was started with the MC146805E2 as the host microprocessor. The further the project went into design, it became clear that the 8k map of the E2 would not be sufficient for all of the required functions. Since a considerable

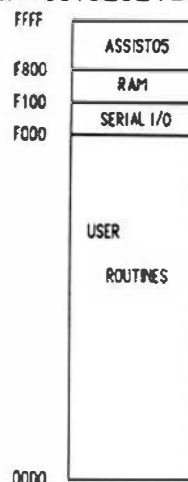
amount of effort had already been spent on software generation, it was not feasible to change host MPUs. Other CMOS MPUs which had an expansion bus were not available either. A simple method of expansion used since the early times of computers was incorporated into the radio. Map switching may be bothersome, but by specifying the entry and exit points of each map as well as parameters removes some of the frustration. Certainly, an MPU with a larger memory map would be desirable.

Enter the MC146805E3

In a second source agreement of transfer of technologies, Motorola received the rights and necessary data bases to manufacture the MC146805E3, a 64k map version of the original E2. The real differences in the two parts are the lack of three I/O bits on Port A. These lines have become A13, A14, and A15.

With most MCU parts, Motorola develops 'monitor' types of programs which allow users to evaluate the MCU without having an expensive development system. The E3 is different, having no on chip ROM since it is an MPU. In an earlier effort, Motorola published the external monitor program 'Assist05', which was used in an expanded MC146805F2/G2 emulator which used the E2 as a host processor. This monitor has been modified for use with the E3, and has some additional capabilities.

The following figure shows the actual memory map of the M146805E3EV8.



Emulation Techniques

There are several different methods which have been used to emulate and evaluate Motorola style Microprocessors. I will describe two methods in this article.

The first method actually provides two memory maps of 64k each. One map is the users, and has no restrictions on its use. The second map is where the monitor ROM, temporary RAM, and serial I/O ports are located. Since a full 64k is available to the monitor, as much ROM may be used as is required, thus providing many functions such as assemblers and disassemblers, multi-level breakpointing and tracing activities. The monitor program provides for two RS-232 ports - one for a terminal, and one for a host computer. Through either of these ports a program may be downloaded into the user's memory map. This users map also has a full 64k map, which allows a program to be placed anywhere.

The heart of this style of system is the map switching logic. Relying on a predictive status line of the MPU which tells the monitor when an op-code fetch is taking place, this logic actually forces a Software Interrupt onto the Data bus. When the interrupt service routine is entered, appropriate action is taken, depending on where the SWI originates (User's code, or by map switch). This type of emulation is done on the M68705, M1468705, M68701, and M68HC11 EVMs. They are called Evaluation Modules rather than emulators because not all chip specifications are truly emulated, and they are of relatively low cost.

The second method, which really cannot be considered true emulation is accomplished by actually taking a 'small' portion of the memory map, using it for monitor routines, temporary RAM, and serial I/O ports. In this type of 'emulation', the user must relocate his code to a lower portion of the memory map. Since the 68XX style of architecture has its interrupt and Reset vectors located at the top of memory, all monitor programs must reside there. Because of this, true emulation cannot be accomplished. Any interrupt service routine will generally have additional time added to it, because of the intermediate jumping which must be directed through temporary RAM.

There are many things which must be considered in the selection of these two different types of systems. First, some MPU/MCUs do not have the necessary lines to determine when to switch maps. This may be accomplished by a sophisticated type of bus monitor, leading to many additional parts such as fast bipolar PROMs and extra 'glue' parts. Certainly, the number of parts is directly related to the cost of the product! This cost is a direct factor on which product is to be used. This article deals with the second type of chip evaluation, and requires very few extra devices. The schematics shown in Figure 2 are all that are required to make the E3 Evaluation Board.

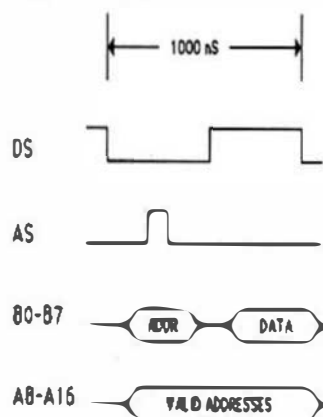
System Operation

The heart of the EVB is the MC146805E3 MPU. The multiplexed Address/Data bus is de-multiplexed by a HC373. This 373 is all that is required to provide a full 16 bit Address and 8 bit Data bus for the user.

Note that only the lower eight address lines are multiplexed with the data bus. This allows the upper eight lines to be used with 'slower' decoding

devices such as PROMs and discrete logic without the worry of propagation delay problems.

Like all 68XX types of MPUs, a synchronous bus is used to transfer data between various I/O and Memory devices. Basically, one signal on the E2/E3 provides system synchronization. This signal is called Data Strobe (DS), and is analogous to the earlier E or O2 signals of the MPU's parent family. During DS low time, addresses are being setup, and other signals are settling. This time period, in conjunction with the Address Strobe (AS) signal, is when the actual bus de-multiplexing takes place.



Although the schematic shows a 5 MHz crystal used in the MPU's oscillator circuitry, the system may be run slower. All Motorola's CMOS and HCMOS computers are fully static, and can be run from DC to full bus frequency. On the E2 and E3, the crystal frequency is divided by 5 to provide the necessary bus frequency. Certainly, if the user requires it, an external oscillator may be used to provide system timing.

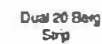
Since the E2/E3 uses a memory mapped technique to address all I/O ports and memory, all external devices must have their own chip select lines. In the E3EVB, these selects are provided by a 256x8 bipolar PROM. A PROM was chosen because it represented the fewest number of chips necessary functions. If more features are to be added to ASSIST05E3, or user routines are to be placed in EPROM, the select table of the PROM may be easily changed to suit the user's needs.

Memory mapped I/O is quite simple to use, as most instructions work with I/O, as well as normal memory instructions. Take for instance the following example which will take one byte of data from RAM, and transfer it to the data register of an I/O port.

```
LDA MEMORY1    Get Data from RAM
STA IOPORT      Put data into the Port
```

The 6805 family, like that of all other Motorola processors use this technique to easily access any type of I/O port or Memory, without having to learn specific I/O types of instructions.

The rest of the schematic is detailed with ROM, RAM, and a MC68681 DUART which provides the dual serial ports. Bus buffers are provided to isolate the users circuitry from the rest of the EVB.



ASSIST05E3

The ASSIST05E3 monitor program is intended for use with the MC146805E3 Microprocessor. The monitor uses an RS-232 link which allows a user to quickly perform both hardware/software development as well as system evaluation. A second RS-232 link is provided for use with a host computer for download capabilities. ASSIST05E3 includes commands which allow for memory and register examination/change, breakpoint set/display, single or multiple instruction trace, a transparent mode for host communications, and a command for downloading from a host computer. The following short paragraphs will explain each command. Also, ASSIST05E3 uses only external RAM for it's temporaries, thus leaving most of the on-chip RAM free for the user.

R - Register Display

The processors registers are displayed.

A - Display/Change the Accumulator

This command begins by printing the current contents of the Accumulator in Hexidecimal, and allows the user to changes it's contents

X - Display/Change the Index Register

This command does the same type of function as the "A" comand, except that it functions on the Index register.

C - Display/Change the Condition Code Register

This command does the same type of function as the "A" command, except that it functions on the condition code register.

P - Display/Change the Program Counter

This command does the same type of function as the "A" command, except that it functions on the program counter. This command is used mainly for tracing.

Breakpoints

Up to three breakpoints may be used to allow debugging of user programs. Program execution may be halted at specified addresses so that the current registers and memory may be examined. Breakpoints set for non-RAM locations will generate an error message. Whenever program execution reaches a breakpoint address, program execution ceases, the current registers are displayed, and the prompt character is returned. Following this, appropriate breakpoint commands may be entered.

B - Display Breakpoints

This command allows all breakpoint addresses to be displayed.

B N XXXX - Set breakpoint N

This command enables breakpoint N, where N is a number 0-2 at address XXXX, where XXXX is the address of the last instruction to be executed.

B N O - Clear Breakpoint N

This command disables breakpoint N, where N is a number 0-2.

Instruction Trace

This command is used to execute one or more instructions, and is generally used after a breakpoint is reached. Tracing may also be used to step through ROM-based programs: however, unlike breakpoints, tracing is not done in real-time. To use the trace command on ROM based programs, the user must put a jump-to-the-ROM entry address in RAM. The user then sets a breakpoint at the jump instruction address. Once the breakpoint address is encountered, the jump is executed and control is returned to the monitor program. The current program counter (PC) then points to the ROM entry address, and tracing may then be used.

T XXXX - Trace Instructions

With this command, XXXX instructions are executed, beginning with the current PC. If XXXX is not specified, only one instruction will be traced, with registers being displayed.

M XXXX - Memory Examine/Change

With this command, all memory locations of the MC146805E3 may be examined and changed.

G XXXX - Execute user Programs

This command allows the user to execute programs which have been downloaded or manually placed in RAM. If XXXX is not specified, the program will begin execution from the current program counter.

H - Host Communications

This command allows communication with a host computer connected to the HOST RS-232 connector. A Control "A" character will return to ASSIST05E3.

D - Download from Host port

This command allows the user to type any character string which will be echoed to the computer connected to the Host port. After a carriage return is entered, ASSIST05E3 waits for the Host to send down S1-S9 records which will be loaded into RAM.

Although the M146805E3EVB with ASSIST05E3 has been constructed with a minimum number of external components, it has capabilities which turn it into a viable development tool. A 40-pin ribbon cable from the bus side of the schematics in Figure 2 to the user's target system is all that is required to allow the EVB to start doing useful

development work. For downloading into the memory map, the user must replace any ROM/EPROM that may be on the target system with RAM, so that S1-S9 records may be downloaded into it.

For systems that require not only CMOS technology, but a relatively large address space, the MC146805E3 may fill the bill for many users.

Versatile Chip Set Puts Overlay In Your Graphics Design

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and

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Many video graphics applications require simultaneous text and graphics to be presented on a display screen that has an external source of video information present. Overlay applications typically occur when a camera, video disk or video cassette recorder output requires additional information to make the picture more useful.

Where are video overlay applications likely to occur? Applications like medical imaging, video micrometry, industrial inspection systems, complex animation, security systems, environmental systems, such as undersea camera work, video printing systems and video disk based recording or educational systems can all use overlay. Each of these systems will place different demands on the text and graphics generating system.

The fundamental problems encountered by designers of microprocessor based overlay graphics systems can be categorized into five major areas: (1) The Microprocessor interface, (2) the memory interface, (3) the video interface, (4) the overlay interface, and (5) the software overhead in generating text and graphics. Additionally, memory bandwidth, CRT limitations, and, of course, performance/price ratio will influence the design.

The solution to this problem is to create a VLSI graphics system in silicon that fixes the hardware architecture, thus minimizing hardware design time, yet allows enough flexibility for the system designer to choose the amount of memory, horizontal and vertical resolutions, the color selection, the choice of microprocessor and the video interface. The next step is to make the system highly programmable so that the design can easily be adapted to a multitude of applications.

The Raster Memory System (RMS) is a two chip set that generates video displays for a full range of performance. The RMS consists

of the MC68486 Raster Memory Interface (RMI) and the MC68487 Raster Memory Controller (RMC). The versatility of the RMS lies in its capability to support many modes of operation with minimal hardware impact and the implementation of software tools in silicon, resulting in a significant reduction in microprocessor overhead in generating text and graphics. A designer starts by defining a hardware system and then proceeds to choose the appropriate video mode. Then the system performance is determined by the choice of microprocessor, the amount of dynamic RAM and the level of sophistication of the software.

Several features have been included into the RMS to ease the designer's task. As shown in Figure 1, the RMI provides the master oscillator for the system. It supplies the RMC with three timing clocks, the microprocessor clock, generates multiplexing signals (ADEN, ADSEL, and DBEN) for display and MPU accesses to memory, provides DRAM address generation including transparent DRAM refresh, and decodes addresses in the memory map other than its own. The additional address decoding brought out on the 3-bit S bus allows chip selection functions to be implemented with a 3 to 8 line decoder, thus providing a system and seven more chip selects for peripherals. The X bus shown in the block diagram is used for address multiplexing as well as a data path for the RMC to communicate with the RMI.

THE MICROPROCESSOR INTERFACE

Since the RMS operates with any of three popular microprocessors—the MC6809E, the MC68008, and the MC68000—the RMI will provide Data Transfer Acknowledge (DTACK) handshaking and a 7.95 Mhz MPU clock if a 68000 family MPU is used or Enable (E) and Quadrature (Q) in a 6809E mode. It is the designers choice to have the Raster Memory System generate DTACK for some or all of the system peripherals. The only requirement is



The other microprocessor interface signals, Address Strobe (AS), Upper Data Strobe (UDS), Lower Data Strobe (LDS), Read/Write (R/W) and Data Bus Enable (DBEN) complete the microprocessor interface. The AS line is a handshaking signal that indicates to the system that the address on the processor bus is valid and that the processor is ready to initiate a machine cycle. UDS and LDS have two functions: The processor uses them to indicate whether the current cycle involves the high data byte, the low data byte, or both, of a 16 bit transfer. The UDS and LDS signals are also used to inform the RMS that the current processor cycle has ended. R/W connect to both chips and informs them of data direction flow on the data bus. DBEN is used by the RMC for gating the MPU data bus onto Ports A and B of the RMC or DRAM.

The system works with several types of dynamic RAMs. A designer can select memory size which can be as little as 16 kbytes in a low end graphics system or as much as 1 Mbyte in the largest system configuration. The type of DRAMs that the system can use are 16k by 1, 16k by 4, 64k by 1 and 256k by 1 and should have a 150 ns access time for proper system operation. The system designer has a choice of one, two, or four banks of DRAM. With a single bank, there will be a loss in performance since the RMS uses the page modes access features of DRAM to improve the data throughput rate. In a 68000 based system, the memory is configured in either two or four banks. Since the memory is not solely

The system operates synchronously to maintain a steady stream of video information to the screen. This basic system timing, called a memory cycle (9 MCLK cycles), imposes limitations on the microprocessor throughput. In a 6809E system, the MPU is run synchronously with this timing, but in a 68000 type system, the RMS adds two wait states (250 nsec each) to every processor memory access. Additionally, the processor will at times request data at an instant that the system is unable to provide it. While these are limitations, it is unlikely that the design will require a faster version microprocessor because the video memory manipulation capabilities of the RMS substantially reduce the microprocessor's overhead tasks.

During each memory cycle, approximately 1 usec, access to DRAM is multiplexed so that the microprocessor and the display process each get one access. In 8 bit bus systems, microprocessors are allowed to read or write one byte, while a MC68000 can access either a byte or a 16 bit word. The number of bytes fetched by the display process will depend on the number of memory banks used and the type of memory cycle the current access requires. Different types of memory cycles are used by the RMS to handle transparent DRAM refresh, fill list buffers, fill object buffers and arbitrate the type of microprocessor memory access. Data called from RAM is latched into the RMC via Port A, shown in Figure 2, (and Port B for 16-bit systems only) with a composite CAS strobe (CASTB) generated by the RMI. This raw data will be internally pipelined and processed until it emerges as analog RGB video signals.

The Raster Memory Controller, shown in Fig. 2, contains all the circuitry for generating the video timing signals. It also generates all display addresses, passing them to the RMI on the X-bus; receives data from memory; processes that information into pel by pel video information; maintains the DRAM refresh addresses, contains all the registers for programming the RMS, and has an on board display Arithmetic Logical Unit (ALU) that performs real time calculations for screen data manipulation.

One of the most difficult problems encountered in a microprocessor/video design is working out all those stringent timing details. In converting digital data to video, the RMI provides a video timing clock (VTCLK), a memory timing clock (MTCLK), and a Pixel clock (PEL) to the RMC as shown in the lower left portion of the block diagram. RMC maintains synchronization with the RMI by providing a horizontal sync (HSYNC) reference pulse back to the RMI. Thus all the video timing is defined for the system designer. The designer sets the mode of operation, NTSC or PAL and 6809E or 68000 family, by simply connecting the appropriate X bus line to the system reset circuitry. The RMS maintains proper signal timing for all aspects of the system by clock stretching MTCLK, if necessary, at the end of a memory cycle and re-synchronizing both MTCLK and PCLK to VTCLK at the trailing edge of horizontal sync. VTCLK is a free-running clock and it is never

re-synchronized, while PCLK and MTCLK have their frequency defined by software selecting the horizontal resolution. PCLK varies from 6 to 14 Mhz, while MTCLK is always the master oscillator divided by four plus any stretching for a ninth cycle of the basic memory cycle.

The RMS has programmable horizontal and vertical resolutions allowing the same program to run on a variety of displays. Assume a program created using a high resolution work station monitor must be displayed on a lower resolution system or a home television. If the virtual screen is defined to be the same on both systems, the same data base can be used. The lower resolution system would simply display less of the data at one time and scrolling could be employed to view all of the original screen. There are four horizontal resolutions, 256, 320, 512, and 640, and up to 10 vertical resolutions, ranging from 192 to 500 lines, offered within the system. Not-interlaced, interlaced sync and interlaced sync and data modes are also software selectable.

applications, it creates many subtly different shades of the same color. In others, it can generate a large selection of divergent colors. With 12 bits defining color, the RMS has a color palette of 4096 colors. The color selection is limited by the mode of operation: 16 colors in bit plane and 32 colors in list modes. True objects use the color mapping RAM somewhat differently in that they include a transparency option and up to 24 different colors for each object.

Another important tool of the system is the virtual screen, which is used when a picture will not fit onto the displayed screen without a loss of detail. In conventional video graphics systems, the programmer stores a complete picture in one section of memory, then transfers a subset of that memory to the screen display memory. The technique allows a operator to pan through the picture, concentrating on individual sections. This continual data movement is microprocessor dead time if it is also burdened with complex calculations while it is trying to do screen management

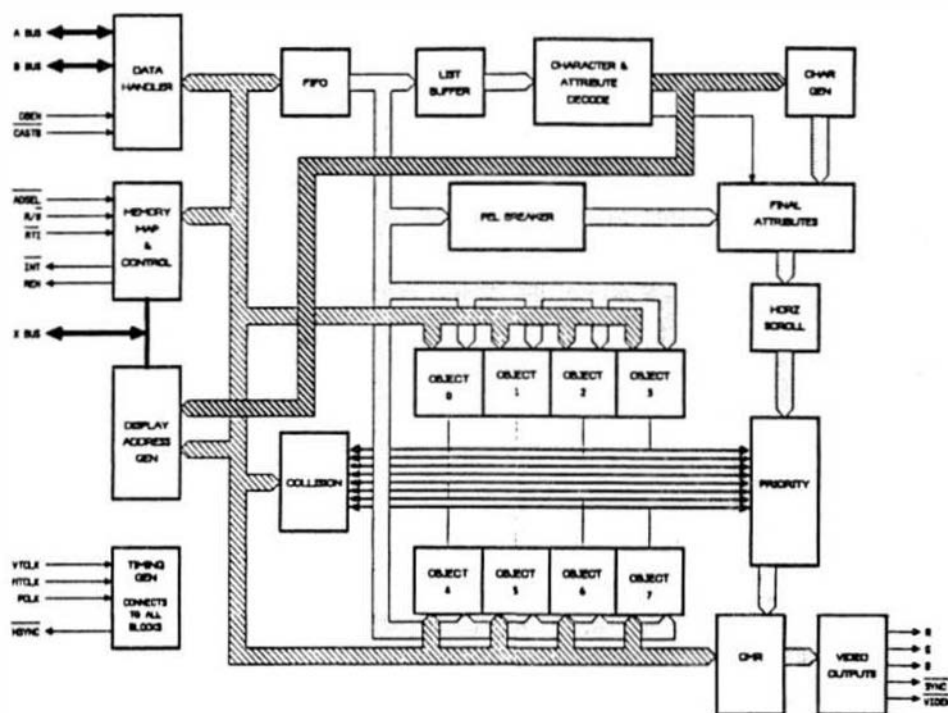


FIGURE 2 RASTER MEMORY CONTROLLER BLOCK DIAGRAM

SOFTWARE TOOLS PUT IN SILICON

All data that is processed within the system results in a 5 bit value that addresses a programmable color look up table or color mapping RAM (CMR) within the final stages of the RMC. The CMRs consist of 32 word locations. The contents of each of these 16-bit locations define a unique color. Twelve of the bits - 4 bits each for red, green, and blue can be programmed directly by the microprocessor. An additional bit within each CMR brought out to the VIDEN pin on the RMC. It is used for pixel by pixel switching capability in overlay applications. The color mapping RAM is a powerful tool for controlling a video screen. In some

functions; not to mention operator frustration each time large amounts of data are moved.

The RMS eliminates the microprocessor overhead for large data block movements by supporting a virtual screen in hardware. In standard systems, hardware defined video memory is scanned in a linear fashion, thus the microprocessor has the burden of adjusting that memory with the correct data. The RMS ALU makes real time calculations for each memory cycle fetch of data, thus the displayed memory does need not be manipulated to do scrolling or paging of data.

To use the virtual screen, a programmer starts by defining the height and width of the virtual screen using a few control registers. Then the display screen size is selected by programming the horizontal and vertical resolution. Finally, the address of where the displayed screen starts in the virtual screen is programmed. Once these registers are set, the programmer now has some scrolling options. For one, he can use the smooth scrolling feature of RMS to pan the virtual screen without having to move any bytes of display data. The RMS offers pixel by pixel scrolling both horizontally and vertically for all display modes. A second option might be to use wraparound scrolling, where the display memory is treated as a toroid. That is, if scrolling proceeds long enough in one direction, it will eventually end up at the scroll start location. Yet, another method of scrolling is to treat the screen as a rectangle. When scrolling reaches a border on the rectangle, the screen is filled with a user defined constant, indicating an off screen event.

SELECT THE CORRECT DISPLAY MODE

In converting memory data to pixels, the RMS supports two basic modes: bit-plane mode, where the user can display individual pels, or six text, character, graphics or games modes called list modes. Additionally, independent of the mode, there are eight identical sets of registers to allow simultaneous independent operation of small X,Y positionable windows called true objects. True objects are hardware intensive objects that move around the screen. They have the capability for collision reporting with fixed or other true objects and priority which allows simulating three dimensional effects all defined in hardware.

In the bit plane mode, data in the virtual screen (and display screen) is converted directly to pixel data. (The screen data is always a CMR address). The programmer has the option of selecting 1,2 or 4 bits per pel which in turn determine whether 2,4 or 16 colors can be used, respectively. Each increase in bits per pel (BPP) results in a doubling of memory requirements; a 320 by 210 resolution screen requires 8.4 kbytes at 1 BPP; 16.8 kbytes at 2 BPP; and 33.6 kbytes at 4 BPP. In the bit plane mode, pixel by pixel independence is obtained at a cost of memory and when more memory must be manipulated the resulting drawing rates decrease.

The list modes of the system were designed to use memory efficiently by giving up some but not all of the pixel independence features. List modes can be thought of as indirect addressing modes, where the data fetched from display memory is used as a pointer to another memory location where the pixel data is stored. The pixel data then contains the CMR address for the pixel color. The same 320 by 210 screen described above can be represented by 3.2 kbytes in list mode 4 with 16 colors. This dramatic reduction of memory results when pixel patterns are well defined, such as text and characters. When pixel patterns are more character oriented, the system allows programming of attributes for further character enhancement.

The list modes were optimized to be oriented toward specific applications. Games and animation applications, text and word processing, mixed text and graphics modes, and graphics modes are all supported.

Attributes or memory size versus performance trade offs are made by simply choosing the right list mode. For example, list mode 0 offers very little in the way of attributes, but its advantage is the small memory requirements because each byte describes one character. In list mode 4, all three bytes describe one character. This mode mixes several types of characters and offers all the RMS attributes that apply to mixed text and graphics applications or games. List mode 5 is designed for high resolution text applications, primarily word processing, but it also has sufficient graphics capability for other applications.

The programmer must be more careful when using list modes because the display memory may not be contiguous. In the list modes, data from display memory for character description will be one, two, or three bytes. When more than one byte is used to define a character, the additional bytes will define attributes, multiple characters, multiple characters with limited attributes or one character with extended attribute capability. All the standard terminal attributes like underline, multiple flash rates, invert, double high, and double wide are supported in silicon. Graphics attributes supported include CMR offset, color/resolution selection, foreground/background color selection, and mosaics 4/6 with separation. The true object attributes include priority, color collision reporting, transparency, independent collision enables, and shading. The attributes used for a display screen are fixed by the list mode used for character attributes, while the true object attributes in general are more independent of mode selection.

Three different types of characters are supported by the RMS: alphanumeric, mosaics and redefinable characters. Alphanumerics are generated by an on-board ROM that appears invisible to the microprocessor. Internal routing on the RMC automatically selects the ROM when required. The additional bytes of decoded display data is routed to the attributes section of the RMC. Mosaics are used to create crude graphics with very little memory requirements. Mosaics are allowed to be either 4 or 6 blocks per character size. Actual size of each of the mosaic blocks may vary from 2 to 5 scan lines in size depending on the size of the character block size selected. Character height is programmable for all list modes with 8,10,12 or 16 lines per character available.

Redefinable characters are essentially RAM based characters that allow a programmer to define a custom set of pixel patterns. These characters have their pixel patterns stored in image tables. The programmer determines the size of each of the patterns, calculates the memory requirements based on the resolution and bits per pel used and stores the patterns in RAM. Memory requirements for each character can range from 8 to 64 bytes. Once the first byte location of the first character is programmed into the RMC, the ALU will make all calculations for the pattern fetches, while the programmer only has to refer to them by number. Thus some of the pixel independence of bit-plane is retained and a much easier method of using them in software is available. To support custom character sets, like Kanji, or specialized graphics characters, the RMS allows creation of up to 32,000 redefinable characters in list mode 2.

True objects are hardware intensive objects that move around the screen. In hardware, they have the capability for collision reporting with fixed or other true objects and priority which allows simulating three dimensional effects. Fixed objects are redefinable characters with additional attributes for interaction with true objects. Objects are defined in image tables like redefinable characters. Moreover, the objects can have a base of 3 colors plus transparency for every pixel and there is color offset allowed for each pixel, resulting in 24 usable object colors. Objects can be defined to be from 14 to 49 pixels wide by 31 lines and can be expanded by hardware zoom by a factor of 1, 2, 4 or 8 in both X and Y directions independently.

Overlay with the RMS the MC1378

To make the RMS operate synchronously with an external video source consider the addition of the MC1378, video overlay synchronizer (VOS), shown in Figure 3. This device contains a complete encoder, i.e.

subcarrier frequency to the VOS. It also controls the Remote/local switch pin for selecting the synchronizing source and the Video Enable pin on the VOS for pixel by pixel switching between the video sources. The vertical/composite pin functions as either an input or output pin depending on the selected mode.

In a local mode, the RMS provides all the synchronizing signals, except the 36 Mhz which the VOS always provides to the RMS. In this case, the RMS provides composite sync via the vert/comp pin. Phase detector 1, PD1, in the VOS (see figure 3) locks the internally counted-down 4 Mhz Voltage Controlled Oscillator (VCO) to the RMS horizontal sync (HSYNC pin). PD2 and PD3 are not used in the local mode. PD4 is active providing an arbitrary phase shift between the color oscillator and the output burst phase. PD5 locks the 36 Mhz RMS clock to the 14 Mhz color oscillator. Therefore the 14 Mhz oscillator is the system standard in the local mode.

In the remote mode, the incoming video

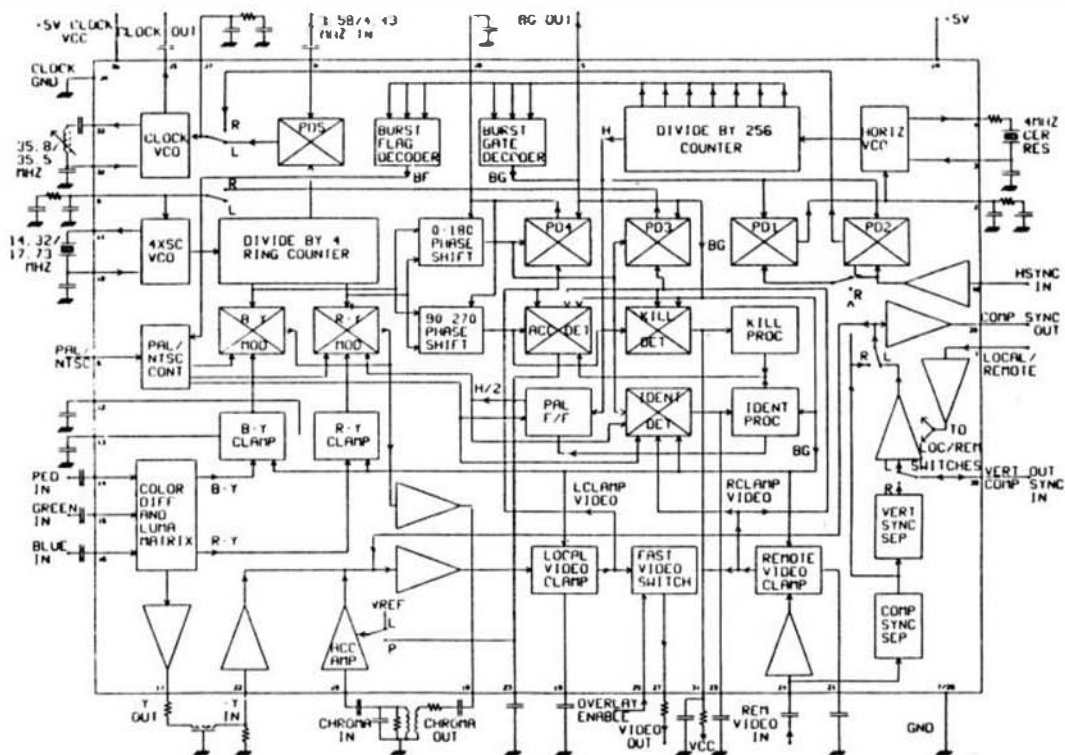


Figure 3 MC1378 COMPOSITE VIDEO OVERLAY SYSTEM

quadrature color modulators, RGB matrix, and blanking level clamps, plus a complete complement of synchronizers to lock the RMS video outputs to any remote video source. It can be used as a local system timing and encoding source for the RMS or it can be used in the overlay (remote) mode.

The block diagram in Figure 4 shows the interface between the RMS and the MC1378. Basic system timing for the RMS is derived from the 36 Mhz oscillator on the VOS. The exact frequency is either 8 or 10 times the color burst frequency depending on whether PAL or NTSC timing, respectively, is used. The RMS provides RGB, Horizontal sync, color

signal supplies all the synchronizing information. A phase lock loop (PLL) is locked to the separated composite sync from the remote signal (PD1, horizontal VCO and 256 divider/counter). This produces a noise protected horizontal reference signal. Vertical lock is obtained by continuously resetting the sync generator in the RMS with a separated vertical pulse also obtained from the external video signal. The 14 Mhz VCO is phase locked to the external color burst frequency using a divide by 4 counter and PD3. Phase detector 4 controls an internal phase shifter (0-180 degrees) to assure that the outgoing color burst phase is the same phase as incoming burst phase. The internal

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- ☐ alphanumeric
- ☐ integer
- ☐ floating point
- ☐ money
- ☐ date

DATA FILE STRUCTURE

- ☐ Packed, fixed length records
- ☐ Memory stored in lower currency unit
- ☐ Data stored as foreign key numbers

INDEXING TECHNIQUE

Sculptor maintains a B tree index for each data file. Program logic allows any numbers of alternative indexes to be coded into one other file.

INPUT DATA VALIDATION

Input data may be validated at three levels:

- ☐ automatic by field type
- ☐ validation list in data dictionary
- ☐ programmer coded logic

ARITHMETIC OPERATORS

- ☐ Unary minus
- ☐ Multiplication
- ☐ Division
- ☐ Remainder
- ☐ Addition
- ☐ Subtraction

MAXIMA AND MINIMA

- ☐ Minimum key length: 1 byte
- ☐ Maximum key length: 160 bytes
- ☐ Minimum record length: 3 bytes
- ☐ Maximum record length: 32767 bytes
- ☐ Maximum fields per record: 32767
- ☐ Maximum records per file: 16 million
- ☐ Maximum files per program: 16
- ☐ Maximum open files: Operating system limit

PROGRAMS

- ☐ Define record layout
- ☐ Create new internal file
- ☐ Generate standard screen form program
- ☐ Generate standard report program
- ☐ Compile screen form program
- ☐ Compile report program
- ☐ Screen form program supervisor
- ☐ Report program supervisor
- ☐ Menu supervisor

RELATIONAL OPERATORS

- ☐ Equal to
- ☐ Less than
- ☐ Greater than
- ☐ Less than or equal to
- ☐ Greater than or equal to
- ☐ Not equal to
- ☐ Logical and
- ☐ Logical or
- ☐ Logical not
- ☐ Logical with

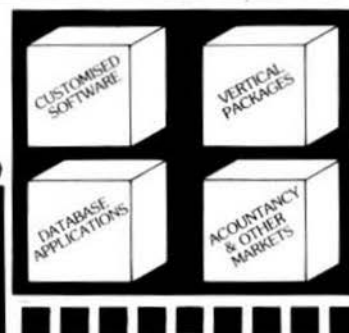
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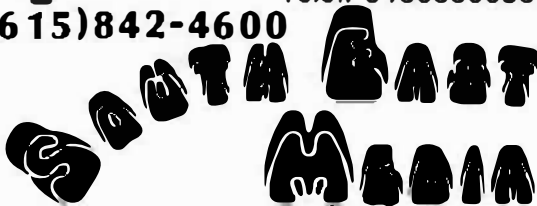
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* Now supplied as a two disk set:

Disk #1: JUST2.COM object file, JUST2.TXT PL9 source: FLEX - CC

Disk #2: JUSTSC object and source in C: FLEX - OS9 - CC

The JTSC and regular JUST C source are two separate programs. JTSC compiles to a version that expects TSC Word Processor type commands, (.pp .sp .ce etc.) Great for your older text files.

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The C source compiles to a standard syntax JUST.COM object file. Using JUST syntax (.p, .u, .y etc.) With all JUST functions plus several additional printer formatting functions. Reference the JUSTSC C source. For those wanting an excellent BUDGET PRICE word processor, with features none of the others have. This is it!

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XDMS System Manual - \$24.95

XDMS Lvl I - F & CCF - \$129.95

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DYNACALC from Computer Systems Center -- Electronic Spread Sheet for the 6809.

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FULL SCREEN INVENTORY/MRP from Computer Systems Consultants -- Use the Full Screen Inventory System/Materials Requirement Planning for maintaining inventories. Keeps item field file in alphabetical order for easier inquiry. Locate and/or print records matching partial or complete item, description, vendor, or attributes; find backorder or below stock levels. Print-outs in item or vendor order. MRP capability for the maintenance and analysis of Hierarchical assemblies of items in the inventory file. Requires TSC's Extended BASIC.

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FULL SCREEN MAILING LIST from Computer Systems Consultants -- The Full Screen Mailing List System provides a means of maintaining simple mailing lists. Locate all records matching on partial or complete name, city, state, zip, or attributes for Listings or Labels, etc. Requires TSC's Extended BASIC.

F and CCF, U - \$50.00, w/ Source - \$100.00

DIET-TRAC Forecaster from Southeast Media -- An XBASIC program that plans a diet in terms of either calories and percentage of carbohydrates, proteins and fats (C P G) or grams of Carbohydrate, Protein and Fat food exchanges of each of the six basic food groups (vegetable, bread, meat, skim milk, fruit and fat) for a specific individual. Sex, Age, Height, Present Weight, Frame Size, Activity level and Basal Metabolic Rate for normal individual are taken into account. Ideal weight and sustaining calories for any weight of the above individual are calculated. Provides number of days and daily calendar after weight goal and calorie plan is determined.

F - \$59.95, U - \$89.95

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O = OS-9, CCO = Color Computer OS-9

U = UniFLEX

CCD = Color Computer Disk

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horizontal reference signal is compared to the H sync signal from the RMI and thus forms a PLL locking the 36 Mhz oscillator such that the horizontal sync has the correct phase relationship. PAL identification is obtained from the subcarrier lock system (identification detector, PAL Flip Flop). The internally generated PAL chroma is then controlled from this identification phase. In the NTSC mode, the identification system is disabled.

Composite Video Generation

The red, green and blue (RGB) analog signals from the RMC are used to generate composite color NTSC or PAL signals. First, color difference and luminance (Y) signals are generated by resistively matrixing RGB. The color difference outputs of the resistive matrix (R-Y and B-Y) then drive two double balanced chroma modulators. The carriers for the modulators are supplied in quadrature from the divide by four ring counter output of the crystal oscillator. The modulator outputs are combined to form the chroma signal and are added to the Y signal along with composite sync to form the complete composite color video signal. In the PAL mode, the R-Y color difference signal changes polarity on alternate horizontal lines.

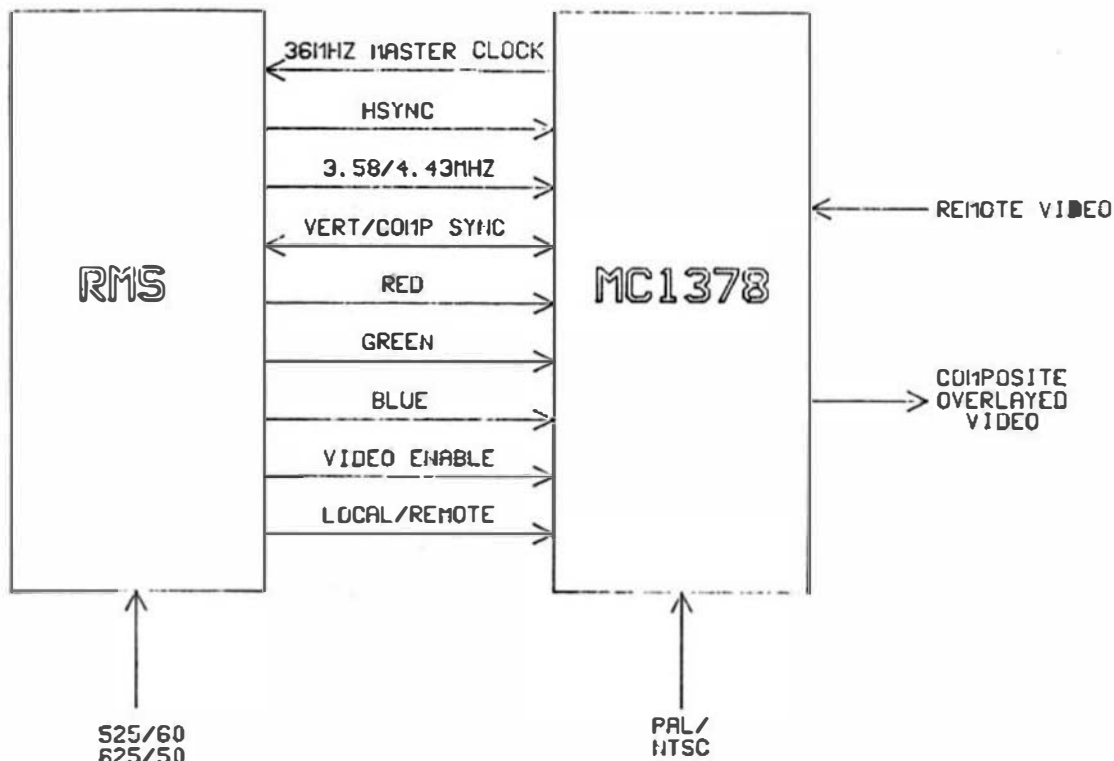
In the remote mode, the phase and the amplitude of the chroma signal is matched to that of the external video signal so that the two composite color signals are completely compatible and may be displayed in an overlay format by operating the video enable change over switch.

Building a RMS based graphics system

A general RMS system based on a MC68000 microprocessor is shown in figure 5. In such a system, the RMS is assigned 1 megabyte of the 16 megabyte address space by decoding the upper four address lines to form a chip select for the RMS. In this basic configuration, the remaining 19 lines, plus Upper Data Strobe, are connected to the system X bus through three 74ALS257 multiplexers. The 20 address lines are time division multiplexed along with RMS memory accesses using only 10 pins.

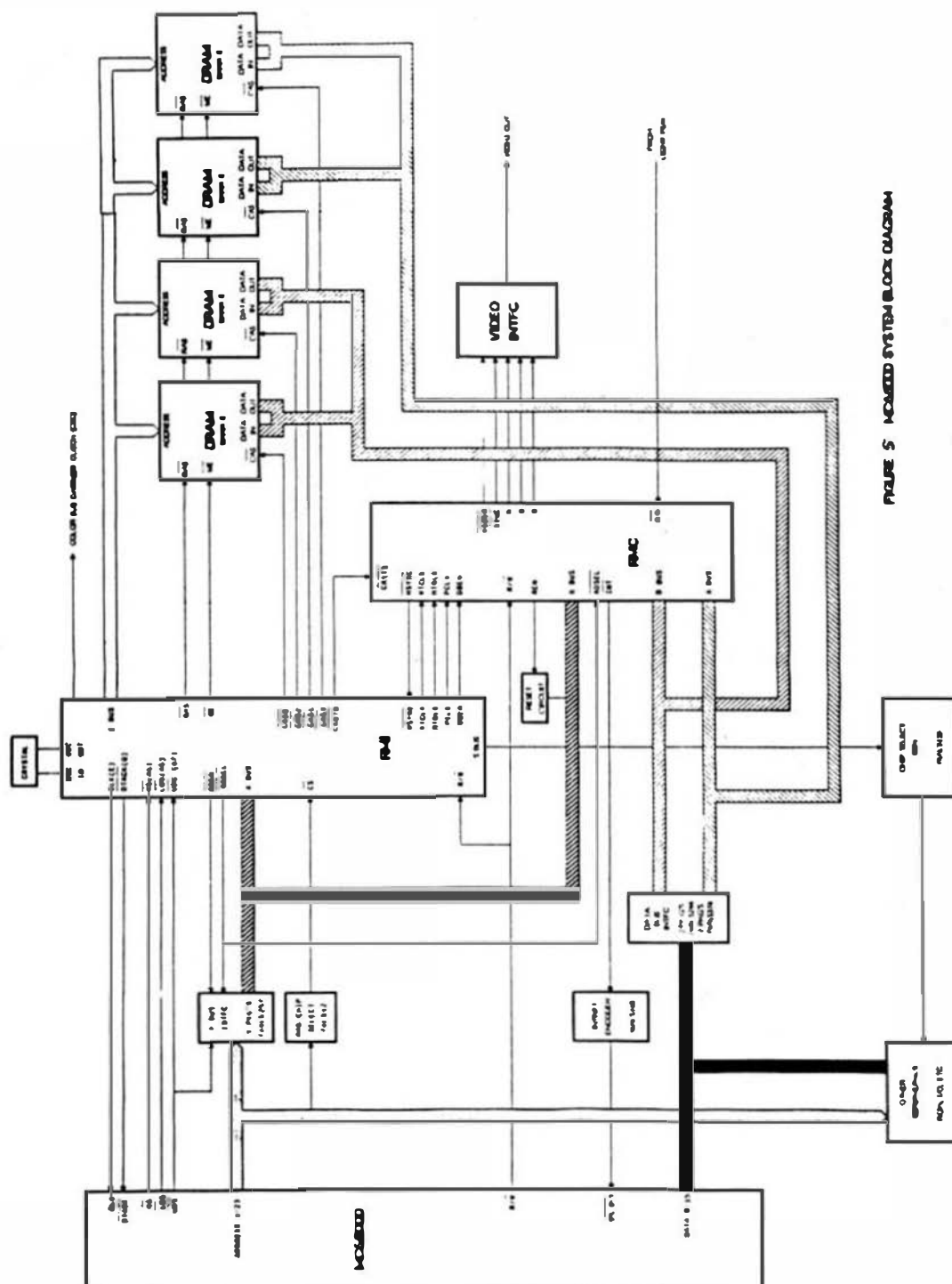
The data bus is interfaced to Port A and Port B of the RMC using two packages of 74ALS244 bus drivers and two packages of 74ALS374 octal latches. The dynamic RAM is organized in byte-wide banks. Banks 0 and 1 are used together to address 16-bit words and separately to address bytes. Banks 2 and 3 are used similarly. Banks 1 and 3 are always the least significant byte of a 16-bit word and are connected to Port A, while the most significant byte, Banks 0 and 2, are connected to Port B.

The system works with a 8 Mhz version microprocessor for which the RMI provides both the clock (7.95 Mhz) and the asynchronous handshake, DTACK. In higher performance applications, the designer may supply a separate higher frequency clock to the MPU, however, access to the RMS will always occur at the RMS rates.



This basic system configuration can be

TABLE 5. MODIFIED SYSTEM BLOCK DIAGRAM



QPL

QPL - A Bold Step to Very High Level Language

This is Part 2 of a series of articles about the QPL programming language. QPL is available for Flex-9 systems from Compiler Products Unlimited, Inc. Phone (602) 991 1657

In the first article, we covered many of the "vanilla" features of QPL; the arithmetic, the compare-branch-a-loop, variable names, and input and output.

In Part 2, we will discuss the pattern matching features of QPL. In the first section of this installment, we will consider the various types of patterns, including alternation, conditional assignment, and Special Patterns. In the second part of this installment, we will look at examples of pattern matching.

PATTERN MATCHING:

What are the applications for pattern matching? In QPL, we use pattern matching to do the following types of tasks:

1. Determine if a string starts with a given pattern of characters.
2. Determine if a string starts with any of several alternate patterns of characters.
3. Determine if a string starts with a given pattern of characters, followed by another pattern of characters.
4. Determine if a string contains a given pattern of characters, anywhere, not just at the start.
5. Extract sub-strings from a larger string.
6. Extract data fields from file records.

In QPL, pattern matching is done by the built-in function MATCH, which takes two arguments; a string, and a pattern. For example, we define STRING1 = "This is a string". To determine if STRING1 starts with "Th", we could write MATCH(STRING1,"Th"). The MATCH function sets the Success/Fail flag which can cause conditional branching as described in Part 1. In the example above, MATCH would succeed. Note that in this pattern match, we have determined that STRING1 starts with "Th", but we do not care what follows. It could be "This" or "That".

ALTERNATES:

It is very common to need to know if a string starts with any of several alternates, for example when interpreting command input in a man-machine-interface situation. To do this kind of pattern-matching, we must create a pattern which contains not only text, but instructions to the MATCH function. Suppose we want to recognize color commands. We would create a pattern of color alternates by the following line:

COLORS = "RED" | "YELLOW" | "GREEN" | U1 | U2 | U3
The pattern COLORS contains not only the values but the

It is very common to need to know if a string starts with any of several alternates, for example when interpreting command input in a man-machine-interface situation.

alternation instruction "|" which is read as "or". Now we have a pattern which can be used to recognize any of six colors. The first three it can recognize are "hard coded" as quoted text literals RED, YELLOW, GREEN. The fourth through sixth colors it can recognize are whatever U1, U2, and U3 contain. For example, we can make U1 = "BLUE". To use the pattern COLORS in a MATCH statement with STRING1, we would write:

MATCH(STRING1,COLORS). As before, if STRING1 started with any of the colors contained in the pattern COLORS, the match will succeed. Now suppose we wanted to know which color in the pattern COLORS matched STRING1. There are two ways of getting this information. One way is by the value returned from match.

VALUE RETURNED by MATCH

The MATCH function returns a value which is the number of the alternate which matched. The first alternate is 0. To use the value returned by MATCH, we would rewrite the MATCH statement above as WHICH_ONE = MATCH(STRING1,COLORS). When we say MATCH returns a value, what it means is that the match statement is replaced by the value it returns. So if STRING1 contains "GREEN", MATCH will return 2, and the MATCH(STRING1,COLORS) part of the statement will be replaced by 2, so that it now reads WHICH_ONE = 2. Obviously, after the complete statement executes, WHICH_ONE will have the value of 2. This tells us which alternate matched.

The other way to determine which alternate matched is by using conditional assignment.

CONDITIONAL ASSIGNMENT:

Conditional assignment means "if this pattern matches, copy what it matched to a variable". In order to perform conditional assignment, we use the conditional-assignment operator, which is a period "." or dot. To use conditional assignment with the pattern COLORS, we would rewrite COLORS as follows:

COLORS = "RED" | "YELLOW" | "GREEN" | U1 | U2 | U3 .
FOUND

Now when we use the pattern COLORS in a MATCH statement, if any of the alternate colors match the value of the string, that part of STRING1 which matches will be assigned to FOUND. If there is no match, the value of FOUND will be unchanged. It is important to note that only that part of STRING1 which matches one of the alternates of COLOR will be copied to FOUND. For

instance, if STRING1 = "YELLOWBIRD", when we perform the MATCH(STRING1,COLORS) then FOUND will contain "YELLOW".

SPLITTING STRINGS:

We sometimes want to split strings for text analysis. For example, suppose STRING1 may contain either "YELLOWBIRDS" or "YELLOWFISH" or "BLUEBIRDS" or "BLUEFISH". We want to determine what color we have, and whether they are fish or fowl. We could do this by making a pattern:

```
ANALYZE = ("YELLOW" | "BLUE") , COLOR & ("BIRDS" | "FISH") , ANIMAL
Now, suppose STRING1 = "BLUEBIRDS".
```

MATCH(STRING1,ANALYZE) will proceed as follows:

```
Try "YELLOW" - no match there
Try "BLUE" - that matches, assign "BLUE" to COLOR.
Resume match scan from end of "BLUE"
Try "BIRDS" - that matches, assign "BIRDS" to ANIMAL
Set success flag and return 0 (the first alternate)
```

In the above example, we split a string based on detailed information about what the string contained. It is often more useful to be able to perform matching when we have less detailed information. To do this, we use the Special Patterns.

SPECIAL PATTERNS:

The Special Patterns are patterns produced by pattern generator functions. These functions are SPAN, BREAK, LEN, SPLIT, ANY, and NOTANY.

LEN:

To use the LEN pattern-generator function we would write a statement like: SP20 = LEN(20). This would generate a special pattern and assign it to SP20. The pattern that LEN generates matches any characters up to the number specified in the LEN argument. Thus SP20 will contain a pattern which matches a run of 20 characters, regardless of what they are. LEN always succeeds (sets success/fail flag to success), except when the string it is matched against is of zero length. LEN patterns with conditional assignment attached are very useful for string splitting. For example,

```
SP20 = LEN(20) . FIRST
creates a pattern which matches a run of 20 characters
and assigns them to FIRST.
```

BREAK:

The BREAK pattern constructor function produces a pattern which will match a run of characters up to (but not including) any character in the BREAK argument. For example,

```
PBRK = BREAK(".,;:")
produces a pattern which matches a string of characters
up to any one of the characters '.,;:'
```

SPLIT:

Sometimes we want to make a pattern which acts like a BREAK pattern, but we want it to stop not on any single character in the argument, but on a sequence of characters. To do

SPLIT PAT = SPLIT("\$A") will create a pattern which will match all characters until it finds the exact string "A". We could use conditional assignment to copy everything the SPLIT pattern matches to a variable. During matching, if the SPLIT argument pattern is not in the MATCH string, the match fails (and conditional

assignment is not done). SPLIT patterns also provide us with a way to determine if a long string contains another string somewhere in it (rather than just at the start).

SPAN:

SPAN produces a pattern which is the logical inversion of BREAK patterns. That is, a SPAN pattern will match a run of characters up until it finds a character which is not in the SPAN argument. SPAN PAT = ("1234567890") creates a pattern which will match a string of characters up until it finds anything which is not a number character. This pattern of all numbers is useful for determining if a string is a numeric integer.

ANY:

This constructor function produces a pattern which matches only a single character, but it may be any one of several characters in the argument. For example, ANY("1234567890") creates a pattern which will match only 1 character, which must be any one of 1234567890.

NOTANY

This is the logical inversion of ANY. It produces a pattern which matches a single character, which must not be in the argument.

APPLICATION EXAMPLES:

Our first application example will be an adventure game.

The game will read a data file named ST1.TXT then present the player with a "room description". It will then ask the player for a "move" command. Depending on which direction the player decides to move, the code will extract a new room from the data file. The room description for the new room will be read from the data file and presented to the player, and so on.

The data file for this simple demonstration program is shown in figure 1. It consists of three "room records".

There may be up to 10 room records in the game data file, with the limit determined by the size of array ROOMS.

In the data file in figure 1, all the text up to the first "\$" is room-description, which the program will read from the text file and display on the screen. The sub-string "\$NX\$SX\$E1\$W2\$" encodes these facts: There are no valid "exits" either north or south. Going east will move you to room 1, going west will move you to room 2. The final "\$" line marks the end of a room record. We will require that this be the only thing on the last line, to simplify the program, and also visually group each room record in the file.

A QPL program consists of data, patterns, and code. We have defined the data, and will next build the patterns we will need.

We will need a pattern which will cause all text up to the first "\$" to be printed in the screen. This "display" pattern will be called DESP PAT. Referring to figure 2, we see that DESP PAT will "match" everything in a string up to "\$" and will assign all it matches to OUTPUT. Remembering that anything assigned to OUTPUT will be printed, you can see how DESP PAT will work.

Next, we will build some patterns which will scan the data and make the room transitions for us. These patterns will be called NORTH PAT, SOUTH PAT, EAST PAT,

and WEST_PAT. Again referring to figure 2, we see that each of these patterns consist of a SPLIT special pattern which will scan to the required part of the room-transition. Following the SPLIT is a concatenated LEN(2) which will scan over two characters (the "SE", etc) in the room transition. Next is a BREAK("\$") which will match all following characters up to the next "\$". Last is a conditional assignment which assigns the left concatenated match (the BREAK("\$")) to NEW_ROOM. Note that conditional assignment is associated to the left concatenated pattern in a compound pattern such as NORTH_PAT. Now with these direction_PAT patterns we have a set of tools which will extract the next-room in a manner which is independent of the number of characters in the room number.

Note that our data file contains delimiter characters ("\$\$") but that it is human-readable file. Also note that no special formatting was required; we did not need leading 0's in the room numbers like 002. The text file can be prepared using an editor, and minimal instructions to the person "writing" the adventure game. Also note that the game itself is completely described by a text file which is external to the game program. In this way we have partitioned the task into two independent sub-tasks, which can be worked on by two people, with little interaction. QPL makes it easy to partition program design tasks because all interactions between QPL programs are in the form of text. Debug is also simplified because people can easily read QPL files.

The next pattern we will need is a command-recognition pattern, called CMD_PAT. Figure 2 shows that CMD_PAT is just a 5-string alternation pattern.

We will design the program in the following manner:

When the adventure program is executed, it will open the data file ST1.TXT and will read each room record into an array. In this way we will have all room "0" data in array element 0, and so on. There is no need for concerns like "will the room record fit in the array element (too many characters?)". Everything always fits in QPL array elements in reading from the file, QPL always reads an entire line, terminated by a carriage return.

The simple "adventure" game of figure 2 is coded for clarity, rather than for small code size. You may notice that the move-patterns NORTH_PAT, SOUTH_PAT, etc., differ by only 1 character, the N,S,E or W. We could write the move-patterns as one generic pattern by replacing the literal "SN", "\$S", etc, with a variable named DIR. The variable DIR would then contain the command that was input (N,S,E,W) with a "\$" prepended using concatenation. This change would allow us to change the MATCH statements at the labels DO_N, DO_S, etc, into a single statement. We would save three lines of pattern definition code, and 3 lines of MATCH code, not counting the labels.

This simple program can be upgraded to a full feature general purpose adventure game program with the addition of about another 70 lines of code. The full feature program utilizes virtual memory techniques to allow the game to be as big as 1000 rooms, with only a 10 element ROOMS Array. We will release the full feature program in a about 1 month.

SUMMARY:

In this simple "adventure" program we have seen that QPL uses data structures which easily accommodate varying types and sizes of data, such as occur in real-world programs. QPL file records are plain text files, which make for easy communication between QPL

programs and programs written in other languages. Extracting data from mixed-data records is easy with patterns containing conditional assignment. These QPL features form a programming language which gets results fast, and produces programs which are easy to modify.

In the next QPL report, we will look at user-defined functions, and some functions which allow us to build large programs from smaller program segments.

```
***** FIGURE 1 - DATA FILE "ST1.TXT" *****
You are standing in a clearing in a woods. To the east is a small
cabin. To the west is a rocky ravine. North and south lead into
dense weedy brush. $NX$SX$Z$W$
```

```
$
This is room 1. $NX$SX$X$W$
$
This is room 2 $NX$SX$X$W$
$
***** END FIGURE 1 - DATA FILE "ST1.TXT" *****
```

```
***** FIGURE 2 - ADVENTURE PROGRAM *****
ARRAY(ROOMS,10)
* First, we build the required patterns.
DESP PAT = BREAK("$") . OUTPUT
NORTH_PAT = SPLIT("$N") & LEN(2) & BREAK("$") . NEW_ROOM
SOUTH_PAT = SPLIT("$S") & LEN(2) & BREAK("$") . NEW_ROOM
EAST_PAT = SPLIT("$E") & LEN(2) & BREAK("$") . NEW_ROOM
WEST_PAT = SPLIT("$W") & LEN(2) & BREAK("$") . NEW_ROOM
CMD_PAT = "N" | "S" | "E" | "W" | "Q"
```

```
* Next, we will read all the room data into the array ROOMS.
OPEN(1,"ST1.TXT",GET,SEQUENTIAL)
RM_NUM = 0
DATA = NULL
READ_LOOP
STATUS = READ(ST1.TXT,STUFF)
* Check to see if we have read to file end.
EQ(STATUS,0) :P(FILE_END)
* Check to see if the line read is the end of the room record.
IDENT(STUFF,"$") :S(HAVE_ROOM)
DATA = DATA & STUFF :(:READ_LOOP)
HAVE_ROOM
* Put the room record into the array ROOMS.
ROOMS(RM_NUM) = DATA
RM_NUM = RM_NUM + 1
DATA = NULL :(:READ_LOOP)
```

* Next, we code the main loop of this simple program

```
FILE_END CLOS(1,ST1.TXT)
RM_NUM = 0
MAIN_LOOP
TEXT = ROOMS(RM_NUM)
MATCH(TEXT,NORTH_PAT)
CMD_LOOP
OUTPUT = "What is your command?"
CMD = INPUT
MATCH(CMD,CMD_PAT) :S(XQT_CMD)
OUTPUT = "I don't understand that command" :(:MAIN_LOOP)
```

```
XQT_CMD
* Here we prepend "DO_" to the move command, so we can do a
* goto-indirect on the value of CMD. '$' is indirection.
CMD = "DO_" & CMD :(:$CMD)
```

```
DO_N
MATCH(TEXT,NORTH_PAT) :(:GO1)
DO_S
MATCH(TEXT,SOUTH_PAT) :(:GO1)
DO_E
MATCH(TEXT,EAST_PAT) :(:GO1)
DO_W
MATCH(TEXT,WEST_PAT)
```

```
GO1
IDENT(NEW_ROOM,"X") :S(NO_EXIT)
RM_NUM = NEW_ROOM :(:MAIN_LOOP)
```

```
NO_EXIT OUTPUT = "There is no exit in that direction" :(:CMD_LOOP)
```

```
DO_Q
* This is the program end. And the "QUIT" exit.
```

```
***** END FIGURE 2 - ADVENTURE PROGRAM *****
```


Bit Bucket

Modem68 Updated

John Moorfoot

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MODEM68 provides for file transfer between two computers using the PLEX operating system, or between a PLEX based machine and a CP/M computer. PLEX utility commands are supported from within MODEM68. The program uses Ward Christensen's protocol for file transfers with Chuck Forberg's YAM batch file transfer mode.

The Christensen protocol is widely used in micro-computer applications and has been well documented in Byte and other journals. The only difference for a header block under YAM and a normal Christensen block is that the header has block number 0. The filename is sent as it appears on the screen in CP/M format and may or may not have a period and extension. The filename is terminated by a null. On completion of file transfer(s) a null filename is sent to terminate the session. For PLEX users, the standard PLEX conventions apply - e.g. .ASM will transfer any files with a .ASM extension, however

due to differences in filename conventions some CP/M filename characters may be translated into an alpha character for FLEX (lowercase z in this version). Also, any CP/M files received without an extension will default to .TXT.

Files of any size can be handled, as there is no requirement for them to fit into memory. The I/O buffer has been restricted to the Christensen protocol block size of 128 bytes for ease of implementation. In practice this does not significantly increase file transfer times, although it may slow things down in terminal mode with data logging.

USAGE:

The program is menu driven and prompts for all input when required. To return to the main menu, (aborting a file transfer) type a ^Z (control Z) from the keyboard. All PLEX utilities obey the same conventions they use normally - e.g. COPY 0 1 will copy all files from drive 0 to drive 1. Switches have been included to provide for batch file transmission, a means of logging all screen display to disk using XON/XOFF protocol, for echoplex operation, to allow proper operation between two computers running PLEX, and to reduce file transmission errors by using cyclic redundancy checking. These switches can be viewed by use of the menu item Z, and may be altered if desired. A carriage return entered in response to the prompt will return to the main menu without displaying the remainder of the switch settings.

DESCRIPTION:

The entire program is written in M6800 assembler code to allow for assembly on FLEX2 and PLEX9 computers.

MODEM68

This is a header file which calls in a number of library files - MOD68-1 to MOD68-11, contains configuration parameters, and has the default settings for the soft switches.

MOD68-1

This file contains all equates used. It also contains some buffer space on page 0 for common variables.

MOD68-2

This is the mainline routine. It prints an initial signon message followed by a menu. All other modes (except return to FLEX) are called as subroutines and return to the menu on completion. Responses to the menu prompts are independent of case.

MOD68-3

All subroutines used by more than one module are contained in this file. There are also initialisation routines for ACIA's used as a modem port.

MOD68-4

Resets the stack pointer and returns to PLEX. This routine also calls the file management system to close any files left open.

MOD68-5

This file contains all file reception stuff. It firstly checks to see what mode is used (normal or batch) and then uses the appropriate routine. Normal mode is fairly straightforward, it prompts for a filename, opens the file and then waits until the line is free to send an initial NAK. Batch mode is mostly concerned with the differences between PLEX and CP/M conventions. Once it gets that all sorted out it calls the normal receive routines until all transfers are completed. You may wish to alter the default compatibility character 'x' in the header file, but this should be set to an ALPHA character, as PLEX requires the first character of a filename or extent to be alpha.

MOD68-6

This routine handles terminal communications mode. If in log mode, you will be prompted for a filename to which all screen data will be logged until you return to the main menu. This mode uses XON/XOFF protocol and is useful for capturing data from bulletin boards etc. When the buffer is nearly full, the system sends an XOFF to halt output from the remote computer. It then waits for a bit to see if anything else arrives before it writes the buffer out to disk. After completion of the write, it sends an XON to restart output from the remote computer. At present, the number of characters positioned left in the buffer before an XOFF is sent is 10. This seems to work ok with an RCPM running at 300bps but may need adjustment for other systems or speeds. If this is the case, change margin in MODEM68.TXT. If the ECHO switch is set, all input from the keyboard is displayed on screen after being sent to line, and anything received from line is returned. Without echo, only characters received from line are displayed. For dialogue between two systems using MODEM68, one must be in echo mode. Also when communicating with a CP/M computer running MODEM or YAM, the CP/M machine must be in CHAT mode or the PLEX machine must be in echo mode.

MOD68-7

This file contains the file transmission bits. Similarly to receipt, the mode is checked first. Much of MOD68-5 (receive file) and MOD68-7 (transmit file) are concerned with the differences between PLEX and CP/M conventions. PLEX allows alpha characters only as the first character in a filename and an extension. It also requires an extension, so the additional characters allowed by CP/M are forced to an alpha character when in batch mode. No attempt has been made to implement file transmission times because PLEX uses space compression, so the amount of data stored is less than that transmitted. The batch send routine uses PLEX filename matching conventions. The code is based on the TSC pdel utility, and performs similarly for name matching, however the filename is accepted from within the program instead of appearing on the command line.

MOD68-8

This routine allows any utility running in the utility command space within PLEX to be

run. It issues the normal PLEX prompt when called, and appears to the user as if he is in PLEX. Any program that runs in low memory must not be executed with this routine - e.g. EDIT. When the utility has completed, it will return to the MODEM68 main menu.

MOD68-9

This routine can be used to abort file transfers from a remote computer.

MOD68-10

This is a routine to display and/or alter switches. Any additional switches should appear in MOD68-1 before endsw and should have a five letter name (including spaces) included in swmsgf in MOD68-11.

MOD68-11

This file contains the command table, all strings and messages and file control blocks and buffers.

MOD68-12

This module contains routines to dynamically reconfigure a 6551 ACIA used as a modem port. You can alter baud rates, number of data bits, number of stop bits, parity, state of RTS, and send a break. Similar functions could be written for a 6850, but baud rate changes are limited.

MOD68-13

Toggles XMODEM mode on/off. This allows you to control a computer running MODEM68 from a remote terminal connected to the modem port. (This could possibly be adapted to a bulletin board system).

MOD68-14

Lists HELP.M68. NOTE: LIST.CMD must be on the system drive, and HELP.M68 must be on the working drive.

ADAPTING TO YOUR SYSTEM:

If you are using a 6850 ACIA for keyboard input and either a 6850 or 6551 ACIA for your modem port, the only changes required will be in the header file MODEM68. Requirements for other systems are discussed later.

One of the operating system equates must be set true, the other false. Set for your system e.g. for FLEX9 set FLEX9 equ true FLEX2 equ false. Similarly set one of a6551 and a6850 true and the other false to reflect your modem chip.

The default switch settings may be changed to suit your requirements. Change to fcb \$ff to turn a switch on. For a description of the switch actions list HELP.M68.

The base address for your modem port and keyboard port must also be set. Also, modem port default parameters should be inserted. For a 6850, ac1 is a master reset and should not need to be changed, ac2 is the control word. For a 6551, acm is the command register and should not normally need changing, ac1 is the control register and should be set for default baud rate requirements. Some values for ac1 are: \$16 - 300bps, \$1a - 9600bps, \$0 - external clock.

A single character to home the cursor and clear the screen is set as ff equ \$c which is a form feed. If your terminal requires more than one character or does not support this feature, it can be set to \$0. This sequence is only used to start the menu at the top of the screen.

The equate to prevent loss of data when logging screen output to a disk file is currently set to 10 in margin. This is the number of characters which can be accepted after MODEM68 sends an XOFF to halt the sending end. If you find you are losing data in LOG mode, increase this value.

As filename conventions differ from CP/M MSDOS/PCDOS to FLEX, a lowercase z is substituted in BATCH mode whenever an illegal FLEX character is discovered. To change to another character, replace the z in the compat equate in the header with another ALPHA character. This is because FLEX only allows alpha characters as the start of a filename and extension.

Users who have other than a 6850 for keyboard input will need to supply their own routine for keyboard status in MOD68-3.T13. FLEX9 users may be able to use the following:

```

kdat jar $cd4e (STAT FLEX call)
  tfr cc,b
  ror b
  ror b
  ror b
  rts

```

The keyboard input routine will also need to be changed, but
 kbdin jar getch
 rts
 should suffice without degrading performance significantly.

Users with devices other than 6850 or 6551 for their modem port will need to write routines for input status, output status, modem input, modem output and port initialization. The requirements for these routines can be found in MOD68-3.T13.

CHANGES FROM VERSION 1.0 to 1.0.4

All user changeable parameters are now contained in the header file MODEM68.TXT. Support for 6551 ACIA's has been added, as has XMODEM mode and cyclic redundancy checking. (The crc algorithm was transcribed from a CP/M module, and I have no idea how it works except that it implements a polynomial - I leave it to those far more mathematically competent to explain). FLEX mode has been added to correctly handle binary file transmission between FLEX computers, and at the same time, inconsistencies in the filename character substitution have been corrected. I have changed the extension of the library files to allow me to quickly locate different versions of a module.

The command loop (MOD68-2) has been changed to alter the prompt for XMODEM mode so that you can tell which end is which when operating remote.

6551 initialization, XMODEM input and output and cyclic redundancy check routines have been added to MOD68-3, and purge has been changed for crc mode. Also, the error routine has been changed to close any files left open when an error occurs. A new routine has been added to check for binary files and to set space compression off if found.

MOD68-4 now includes a call to reset I/O vectors which may have been modified by XMODEM.

MOD68-5 has code added to check for binary files. A problem with timeouts in non-batch mode has been corrected, and crc checking has been included.

In MOD68-6 an alternate return to main menu character ^X has been added to terminal mode to allow a user to escape from terminal mode in XMODEM.

Binary file handling and crc checking have been included in MOD68-7.

Additional code in MOD68-8 is to prevent changing XMODEM mode after executing a FLEX utility.

MOD68-11 has additional tables and messages to support the new routines.

IN CASE OF TROUBLE:

I welcome any suggestions or bug reports. Also any enhancements (such as CRC checking) are encouraged.

N.B. FLEX is a trademark of Technical Systems Consultants. CP/M is a trademark of Digital Research, MSDOS is a trademark of Microsoft, and PCDOS is a trademark of IBM.

*The updated version of MODEM68 is now 68' Micro Journal Reader Service Disk #12. See page 62 this issue for details on how to order.



Art Weller

PASC is the product of:

Mr. Hugh Anderson
 109 Aro St.
 Wellington, New Zealand

As implied by its name, PASC is a Flex9 compiler with a definite Peccol's "flavor", and anyone with a bit of Pascal experience should be able to begin using PASC to good effect in short order. A page in the manual explains the differences succinctly:

"PASC has a block structure similar to PASCAL, although PROCEDURES may not be nested.

PASC doesn't have

TYPES, RECORDS, SETS, FILES
 Multi-dimensional arrays
 Array lower bound specifications
 More than 2 lexical levels
 Assignment of structures larger than 16bits
 GOTOS
 REALs
 A FOR - loop
 The WITH statement
 IO - i.e. the WRITE or READ statements

PASC does have

Easy (UNCONTROLLED) access to memory addresses
 INTERRUPT procedures
 Constant Arrays (The DATA declaration)
 A CODE statement to allow inline insertion of machine code
 ORC and STACK directives

In addition, pointers and strings are different, and call-by-reference is done by hand."

This list of reserved words (keywords) will give a better indication of the scope of this compiler:

AND	ARRAY	BEGIN	BYTE
CASE	CODE	CONST	DATA
DO	ELSE	END	EXTERNAL
FORWARD	FUNCTION	IF	INCLUDE
INTEGER	INTERRUPT	MODULE	NOT
OF	OR	OTHERWISE	PROGRAM
PROCEDURE	REPEAT	RETURN	THEN
UNTIL	VAR	WHILE	XOR

The otherwise excellent manual does not discuss about 1/4 of these, but presumes that the user has had prior experience with Pascal. In a way, that's a shame, for PASC would provide an excellent introductory compiler for a first-time user. It should also be noted that PASC is an "integer-only" implementation, a limitation not in keeping with the rest of its capabilities. The addition of REALs would greatly enhance its utility.

The good news is that PASC departs from the usual practice of providing a run-time-interpreter for the compiled output and instead generates ROMable, relocatable, reentrant native (6809) object code; far more compact and significantly faster. (As Hugh Anderson says, "Who would bother writing any other sort (of compiler) for the 6809?"). In fact, the "run-time package" consists only of the tiny integer arithmetic. This aspect and the fact that there is provision for easy access to RAM addresses and programmer control over DRG and STACK makes it a good choice for the design of utilities, system software, or ROMable code. No command line options are provided, but compiler directives may be included in the program file to control the type of output (source listing, assembler output, binary, and a "debugging" feature). The assembler output would, of course, allow optimizing some critical portion of the program where the use of CODE is inappropriate.

PASC uses rigid syntax and structure (as does Pascal). Careless typlants like me usually have a bit of debugging to do on new programs because of syntax errors while concentrating on the flow of the program. PASC is unforgiving of these errors, stopping dead in its tracks on each one. This isn't quite as bad as it sounds, since many of the compilers that list out all the errors in one run actually get "sick" after the first one or two so that the later ones become meaningless.

In hope of taking some of the pain out of this, the PASC set includes a syntax/structure editor called ED. It makes no pretext about being useful as a text editor, and cannot be, since it is based on a table of the language keywords and attributes. The purpose is to guide the programmer in producing perfect source code (in the syntax/structure sense, that is) -- i.e. the use of ED in entering the program will result in no compile time errors due to these causes.

I found the concept and implementation of ED fascinating; to the point of spending more time learning ED than PASC. And it does, in fact, constrain the programmer to the requirements of the language. A detailed explanation would take too much space here, but some ideas can be gained by visualizing a tree-like arrangement representing syntax required in the use of each keyword. ED allows (requires) tabbing through the tree-structure to find the particular "branch" that is needed, and at each of these points (nodes) it is possible to expand or contract the display to examine the options available at that point. Note the use of the word "constrain" above. While the basic idea seemed a splendid one, the way ED interfaces with its user is tedious, to say the least. The mechanics of using ED are so distracting that I found myself concentrating on use of the editor rather than the program I was trying to work on. However, I can see a great deal of potential in this technique and hope further development effort goes into improving it, since it could be used as

a programming tool for other languages as well. In fact, ED came with a file to convert to Pascal use.

The review disk came with a couple of "freebee" programs (not copy-righted, that is) that should be mentioned. The CHESS source would give some good examples of the use of PASC, but being incomplete, is not of much use in actually playing the game.

There is also a screen oriented EDITOR based on an earlier "C" version that appeared in the Jan '82 Dr. Dobbs. Since it includes the ability to use some of the features of "smart" terminals, I found its screen handling of scrolls, inserts and deletes to be the fastest I've ever used. A really nice editor that became comfortable to use very quickly and has the minimum essential text editing features -- in fact, I'm using it to prepare this review. Curiously, there are no copy or move commands.

By the way, all these programs came with source, including the PASC compiler. A dedicated customizer could have a ball with these.

Art Weller

Editor's Note: PASC is available from S.E. MEDIA. See advertising this issue.

TO THE EDITORS OF 68' MICRO JOURNAL

DEAR SIRS,

HEREWITH I SEND YOU 2 NEW FLEX-UTILITIES.
MAYBE THEY COULD BE PUBLISHED IN YOUR MAGAZINE.

- 1) "RPTERR"
THIS AN OVERLAY TO IMPROVE THE "RPTERR"-ROUTINE OF FLEX. NORMALLY FLEX DOESN'T PRINT THE FILENAME WHEN "RPTERR" IS CALLED; BUT THIS ROUTINE DOES!
- 2) "PRIORITY"
WHEN YOU DEFINE: ASN B=A, FLEX SEARCHES THE DRIVES ALWAYS IN THE SAME ORDER: 0,1,2,3.
WITH THIS OVERLAY, WHICH IS ALSO A COMMAND, YOU CAN CHOOSE YOURSELF IN WHAT ORDER THE DRIVES MUST BE SEARCHED. FOR INSTANCE, IF YOU HAVE A MEMORY-DRIVE AT DRIVE#2, THEN SAY: PRIORITY,2,0 COMMANDS WILL BE SEARCHED FIRST ON MEMORY-DRIVE, AND IF NOT THERE ON DRIVE#0.
YOU CAN GIVE AS MANY DRIVES'S YOU WANT, WITH A MAXIMUM OF 4.

BOTH PROGRAMS WERE WRITTEN FOR FLEX09 V3.1

ETIENNE FRANCOIS
DR.M.L.KINGSTR.61
1121 CR LANDSAEER
HOLLAND

RPTERR.TXT

```

*
FREE EQU $7000 JUST AN EXAMPLE
*
* PATCHES FOR IMPROVEMENT OF "REPORT ERROR"
*
RSETIO EQU $CD2A
ERRTYP EQU $CD20
PSTRNG EQU $CD1E
PUTCHR EQU $CD18
*
*
* PATCH "REPORT ERROR" ROUTINE TO THE NEW ROUTINE....
ORG $D283
JSR RPTERR
*
*
* PATCH "NOT FOUND" ROUTINE TO BE ALSO TO "REPORT ERROR"
ORG $D207

```



```

NOP
NOP
NOP
0
ORG FREE SOME FREE MEMORY (DRIVERS, SPOOLER ETC...)
0
BAVFCB RMB 2 SAVE CURRENT FCB
0
PRTERR STA ERRTP
STX BAVFCB
JSR RSETIO
LDX 0TXER
JSR PSTRNG
0 PRINT FILE NAME FROM FCB AREA (FCB+4)
0 BE CAREFUL, IT MAYBE DAMAGED, BUT SOMETIMES
0 THERE'S COPY AT FCB+36; CHECK THAT ONE TOO!
0 IF BOTH FILENAMES ARE DAMAGED PRINT ALL ?'S.
LDX SAVFCB
LEAX 4,X POINT TO FILENAME 1
LDB 02 CHECK TWO FILENAMES
0 CHECK FILENAME 1 OR 2
CHNAME LDA 0,X CHECK FIRST CHAR OF FILENAME
CMPA 0'A
BCS DAMAGE <"A" IS NOT OKE
CMPA 0'Z
BLS PRTER1 <"Z" IS OKE
DAMAGE DEC0
BEQ NNAME
LEAX 32,X POINT TO FILENAME 2 (FCB+36)
BRA CHNAME
0 BOTH FILENAMES DAMAGED; POINT TO ALL 7???
NNAME LDX 0DQUES ALL 7???
BRA PRTER2
0 IF FILENAME IS OKE...
PRTER1 LEAX -1,X POINT TO DRIVE0
LDA 0,X GET DRIVE0 FROM FCB
CMPA 03 CHECK DRIVE0 IS REAL
BHI NNAME IF DRIVE0 NOT >0 OR <=3
PRTER2 LDA 0,X+
ADDA 0030 MAKE DRIVE0 ASCII
JSR PUTCHR PRINT DRIVE0
LDA 0'
JSR PUTCHR
LDB 00 PRINT FILENAME
JSR PRT
LDA 0'
JSR PUTCHR
LDB 03 PRINT EXTENSION
JSR PRT
LDX SAVFCB
LDA ERRTP
RTS CONTINUE FLEX
0
TXER FCB 07
FCC "ERROR WITH: "
FCB 04
DQUES FCB "?-030
TXQUES FCC "?????????" FILENAME
FCC "???" EXTENSION
0
PRT LDA 0,X+ GET CHAR FROM FILENAME
BEQ PRT1 DONT PRINT 000
PRT2 JSR PUTCHR
PRT1 DEC0
BNE PRT
RTS
0
END

```

PRIORITY.TXT

```

0 PRIORITY.CMD
0 SET PRIORITY OF DRIVES IF ABN 5=ALL
0
0 FORMAT 1: PRIORITY (shows current priority)
0 FORMAT 2: PRIORITY.CMD,[drv1],[drv2],... (max.4)
0 FORMAT 3: PRIORITY.CMD,[drv1][drv2],... (max.4)
0 (comm's omitted)
0
0
0 PROGRAMMED BY ETIENNE FRANCOIS
0 LANDMEER, HOLLAND
0
PSTRNG EQU 0CD1E
TCHR EQU 0CD15
MARKS EQU 0CD03
SYSDRV EQU 0CC0B
ORVBEL EQU 0DE0C

```

```

PUTCHR EQU 0CD10
NXTCH EQU 0CD27
LAST EQU 0CC11
TTYEOL EQU 0CC02
DRVRDY EQU 0DE0C DRIVE READY FLEX
0
0
ORG 0C100
0
PRIORT BRA PRIORTT
0
VN FCB 9 23/03/85 E.FRANCOIS
0
COUNT RMB 1
TABPOI RMB 2
0
0 INIT DRIVE COUNTER & PRIORITY-TABLE POINTER
PRIORTT LDA 0031
STA COUNT
LDX 0PRITAB
STX TABPOI
0
0 LOOK FIRST IF DRIVE0'S WERE GIVEN IN COMMAND-LINE
0 SET THESE DRIVE0'S FROM COMMANDLINE AND PUT
0 THEM IN PRIORITY-TABLE.
0
0
PARAB LDA LAST
CMPA 0000
BEQ PRINT NO DRIVES SPECIFIED; PRINT CURRENT PRIORITY.
CMPA TTYEOL
BEQ PRINT BARE....
0
0 INIT PRIORITY-TABLE (4 ENTRIES + END-OF-TABLE)
0
INIT LDX 0PRITAB
LDB 05
INI1 LDA 00FF
STA 0,X+
DEC0
BNE INI1 NEXT TABLE ENTRY
0
0 GET THE DRIVE0'S FROM CMDLINE
PAR1 JSR NXTCH
CMPA 000
BEQ STOP
CMPA TTYEOL
BEQ STOP
CMPA 0020 SPACE?
BEQ PAR1 SKIP IT
CMPA 0', COMMA?
BEQ PAR1 SKIP IT ALSO
0 SO ASSURE IT'S A NUMBER NOW....
SUBA 0030 CONVERT DRIVE0 FROM ASCII TO HEX
LDX TABPOI
STA 0,X+ PUT DRIVE0 IN PRIORITY-TABLE
STX TABPOI UPDATE TABLE POINTER
SKIP LDA COUNT
CMPA 0034
BCS PAR5 IF <
DUPPY JSR NXTCH READY; 4 DRIVE'S SPECIFIED;
READ UNTIL 0D OR TTYEOL
0
CMPA 00D
BEQ STOP
CMPA TTYEOL
BEQ STOP
BRA DUPPY
0
PAR5 INC COUNT
BRA PAR1 GET NEXT CHAR; IF THERE'S ANY...
0
0 SET SYSDRIVE TO "SEARCH ALL" (S=A)
STOP STA LAST
LDA SYSDRV
LDA 00FF
STA SYSDRV
0
EXIT JMP MARKS
0
0
PRINT LDX 0PRITAB CHECK IF AT LEAST 1 PRIORITY
0 WAS GIVEN
LDA 0,X
CMPA 0003
BLS PRINT2 PRIORITY IS DEFINED; PRINT IT
JMP NOPRIO NOT DEFINED; PRINT WARNING
PRINT2 LDX 0TXPRI
JSR PSTRNG
LDA 05 MAX. 4 DRIVES
STA COUNT
PRINT1 LDX TABPOI
LDA 0,X+
STX TABPOI
DEC COUNT
BEQ EXIT MAXIMUM 4 DRIVES!!

```



```

COPA e$FF
REQ EXIT
ADDA 0030 WAS HEX; MAKE ABCD
JSR PUTCHR
LDA 0020 SPACE
JSR PUTCHR
BRA PRINT1
TXPRI FCC "CURRENT PRIORITY: "
FCB 4
$
NOPRI0 LDX 0TXNOPR
JSR PSTRNG
JMP WARR0
TXNOPR FCB 0D,0A,0A
FCC "PRIORITY WAS NOT YET DEFINED!!!!"
FCB 0D,0A
FCC "DEFINE IT LIKE THIS: PRIORITY,0,1"
FCB 0D,0A,4
$
$
$ PATCHES FOR PRIORITY ROUTINE; REPLACE OLD FNDNXT
$
ORG 0DD8D OLD PLACE OF FIND NEXT READY DRIVE ROUTINE
$
$
FNDNXT LDX 0D40B - FCB ADDRESS
LDA 3,X
LDX 0PRITAB
TSTA LOOK IF FIRST TIME
BMI YES DRIVEe = OFF
NO TST 0,X
BMI NFOUND END OF TABLE
COPA 0,X
REQ FNDNXT
NEXT LEAX 1,X
BRA NO
FOUND LEAX 1,X
YES TST 0,X
BMI NFOUND
OKE LDA 0,X
LDX 0D40B
STA 3,X PLACE IN FCB
JSR DRVDRY
BCS FNDNXT DRIVE NOT READY; NEXT DRIVE
RTS
$
NFOUND LDX 0B40B
LDB e$10 FORCE ERROR
SEC
RTS
$
$
$ PRIORITY TABLE
$
PRITAB RMB 5
$
END PRIORT

```

PT-69 OS-9

Last year I reviewed several SBCs. One was the PERIPHERAL TECHNOLOGY PT-69 SBC. As you might remember I felt that this was one of the better systems. Well, after a year or so of heavy use, I still feel the same way about this system.

This was one of the SBCs that I installed in a Heath H19 CRT terminal. This system has two 40 track drives. Eighty track drives could be used. It has performed flawlessly and not one bit has ever been lost running FLEX/STAR-DOS. However, as more of our applications are being developed under OS-9, I decided to install the PT-69 OS-9 system.

The PT-69 is designed so as to only run FLEX/STAR-DOS or OS-9. A monitor EPROM is furnished for each system. Conversion from one to the other is simply changing the EPROMs, maybe one or two other simple circuit changes, and away you go. Fact is, it is so simple to change that the complete installation instructions are only one page.

After installing the EPROM a jumper must be changed from the 271b position to the 2732 position. And if your board is an older one, PT-69 or PT-69-1 you will have to install one wire if you intend to run a Centronics type printer. Also some of the very earliest boards will require one resistor change. And that is it.

Standard level one logical devices are supported /DO, /DI, /TERM, /TI, /P, and /PI.

Available as an option is a CoCo disk driver and device descriptors. Also an upgrade package is very reasonable (\$30.00) for those wishing to upgrade older systems to the latest, including the CoCo disk routines and new EPROM. For an additional \$15.00 the factory will upgrade your board also.

One very nice feature of this board is a battery backed up time of day system clock. I hate to type in the date and time everytime I fire up. Like the big systems, this one does it for you.

For the person wanting to get into OS-9 and wanting more than a color computer but not the price of some of the other systems, this one is a winner. It is a full blown OS-9 level one system. It easily supports two users in multi-user mode, or allows several applications run in background and interactive at the same time. The cost of our system breaks down as follows:

Used Heath CRT Terminal	\$250.00
PT-69 SBC	279.00
OS-9	200.00
2 40 track drives (used)	150.00
Total Cost	\$879.00

Mind you, this is all of it, including a very nice 80 character by 25 line CRT terminal. For those already having a CRT, then I would suggest one of their system packages, either floppy or hard disk. The price is hard to beat, and the quality is there. Also we have had remarks from readers commenting on the cooperation received from their phone calls, letters, etc. It is a nice feeling to know that some vendors really do care.

Please see their advertisement this issue.

--

B-A Bergvall, Muskvarna, Sweden, 86-04-06.

A BOOLEAN EPROM PROGRAMMER.

or

The poor man's PLA programmer.

In a hardware project I needed a general boolean random logic section. The natural choice would have been a PAL programmable logic device. But, I have neither a PAL programmer nor PAL programming software.

However, an EPROM can perform the function of an unregistered PAL. In fact, the PAL is only a subset of the EPROM. In the PAL only a limited number of product terms can be programmed, but in the EPROM all input combinations are available for programming, each corresponding to one input address.

One disadvantage of the NMOS EPROM is its slow speed, typically 200 to 450 ns, compared to the bipolar PAL 20 to 30 ns. Fortunately, the speed in my application is not very critical, and a 450 ns 2716 NMOS EPROM is speedy enough.

But, how do I program it to solve my boolean equations? I have an EPROM programmer but have never heard of any boolean EPROM software. So I created it, using Basic09 and my Prime1 PD2000 OS9 computer.

First I named the EPROM inputs and outputs to application specific names. The program "boolrom" was then edited and run to make the EPROM pattern file "eprom1". This file was

copied to the EPROM using my EPROM programmer. The EPROM was inserted into the circuit, completing the EPROM design cycle.

The description below is tailored to my application, but I have tried to make the documentation very explanatory. You can use my program "boolrom" as a template to create your own programs for your combinatorial needs. Just replace my variable names with yours and rewrite the Conditional section with your algorithms.

My 2716 EPROM is used in an application with a step motor and two solenoids and is configured according to Drawing 1. The 2716 has 11 address inputs and 8 data outputs, all used in the application.

The six LSB inputs are connected to a counter, and these inputs form one common integer variable named "count". The remaining five inputs and the eight outputs are used independently and each have a separate boolean variable with its own name.

The allowed mixing of variable types simplifies the algorithm design considerably and illustrates the flexibility of this EPROM programming method. You can think of the added labor involved in specifying the input conditions of the separate counter inputs for the many different counts that are used in the application. When programming PALs you normally have to do that exercise.

Most of the EPROM outputs are fed to flipflops. This causes a problem because the outputs can carry glitches from input transitions causing the flipflops to misbehave. You might consider using another EPROM input as a gating clock. But the EPROM's individual input behaviour is not revealed on the manufacturers' data sheets. An EPROM clock input can consequently not safely gate off other inputs.

Thus don't use internal clock gating but instead use external clock gating at the outputs to protect flipflops. This is a drawback compared to PALs which produce no glitches when a gating clock is off.

The "boolrom" program is mostly selfexplanatory. It analyses one input address at a time. Each address corresponds to one input combination. For each address the program finds the corresponding values of the input variables. The Conditional section uses IFs, ANDs and ORs on the input variables to create the output variables. The output variables are then collected to an output data byte, which constitutes the data content of that particular input address. The data byte is written to the pattern file "eprom1".

The above process is repeated for each input address until the complete address field of the EPROM is covered. The process will take some minutes. The process is slowed down by the repetitive use of power-of-2 expressions. These are used to make the program easier to understand but can be replaced by implicit integers to speed up the process.

```

0000 REM ***** boolrom *****
0001 REM *****
0002 REM *****
0003 REM *****
0004 REM *****
0005 REM *****
0006 REM *****
0007 REM *****
0008 REM *****
0009 REM *****
0010 REM *****
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0099 REM *****
0100 REM *****
0101 REM *****
0102 REM *****
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0201 REM *****
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0232 REM *****
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0240 REM *****
0241 REM *****
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0249 REM *****
0250 REM *****
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0255 REM *****
0256 REM *****
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0301 REM *****
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0697 REM *****
0698 REM *****
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0700 REM *****
0701 REM *****
0702 REM *****
0703 REM *****
0704 REM *****
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1000 REM *****

```

```

0121 DIM A10:BOOLEAN
0122 DIM direction,delayerdirection,steporder,stepreset,reset:
0123     BOOLEAN
0124
0125 REM Output variables:
0126 DIM databyte:BYTE
0127 DIM D1:BOOLEAN
0128 DIM inamp1,pull,stepresponse,resetstep,forward,motorstep:
0129     BOOLEAN
0130 DIM limit,enable:BOOLEAN
0131
0132 REM Auxiliary variables:
0133 DIM i,j,k,l:INTEGER
0134
0135 REM File variables:
0136 DIM file:BYTE
0137 DIM filename:STRING
0138
0139 REM ***** OPEN AN EPROM PATTERN FILE: *****
0140 filename="eprom1"
0141
0142 REM Overwrite possible old pattern file:
0143 ON ERROR GOTO 100
0144 OPEN file,filename:WRITE
0145 ON ERROR
0146 GOTO 110
0147 ON ERROR
0148 CREATE file,filename:WRITE
0149 REM "Landing point" is old file exists.
0150
0151 REM ***** CREATE THE EPROM PATTERN: *****
0152
0153 REM number of input bits:
0154 inputbits=11
0155 BASE 0
0156
0157 REM ***** Analyse at a time one input address *****
0158 REM s - one input combination -
0159 REM s - one output byte.
0160 FOR address=0 TO 2^inputbits-1
0161
0162 REM i=leftover of current input address
0163 REM j="mark" of particular input address bit
0164 REM k=bit number of particular input bit
0165 l=address
0166
0167 REM Find the input variables A(inputbits-1) to A(0) at the address:
0168 FOR k=inputbits-1 TO 0 STEP -1
0169
0170 REM Special: Catch the counter count at A(5)
0171 IF k=5 THEN
0172     count=1
0173 ENDIF
0174
0175 i=2^k
0176 IF i>=1 THEN
0177     A(k)=i
0178 ELSE
0179     A(k)=FALSE
0180 ENDIF
0181 NEXT k
0182
0183 REM Assign the input variables:
0184 reset=NOT(A(10))
0185 delaydirection=A(9)
0186 steporder=A(8)
0187 delayreset=A(7)
0188 direction=A(6)
0189
0190 REM A(13) A(0) carrying 4-bit counter value "count".
0191 REM inputs available but not used as boolean.
0192 REM A(13)=MSB, A(0)=LSB.
0193
0194 REM ***** The Conditional (boolean) section determining
0195 REM the output variables from the input variables.
0196
0197 REM Default outputs, used when no specific value is assigned:
0198 pull=FALSE
0199 stepresponse=FALSE
0200 resetstep=FALSE
0201 forward=TRUE
0202 motorstep=FALSE
0203 limit=FALSE
0204 enable=FALSE
0205
0206 REM In all cases:
0207 inamp1=COUNT
0208
0209 IF reset THEN
0210     resetstep=COUNT
0211     limit=COUNT<=16 OR COUNT=30
0212     enable=COUNT>=60 OR COUNT=0
0213 ENDIF
0214
0215 IF steporder AND NOT reset THEN
0216     IF direction THEN
0217         pull=COUNT>=30 AND COUNT=61
0218     ELSE
0219         REM reverse:
0220         pull=COUNT<=16 AND COUNT=30
0221     ENDIF
0222     resetstep=COUNT
0223     stepresponse=COUNT
0224     REM stepdir stepping
0225     forward=direction

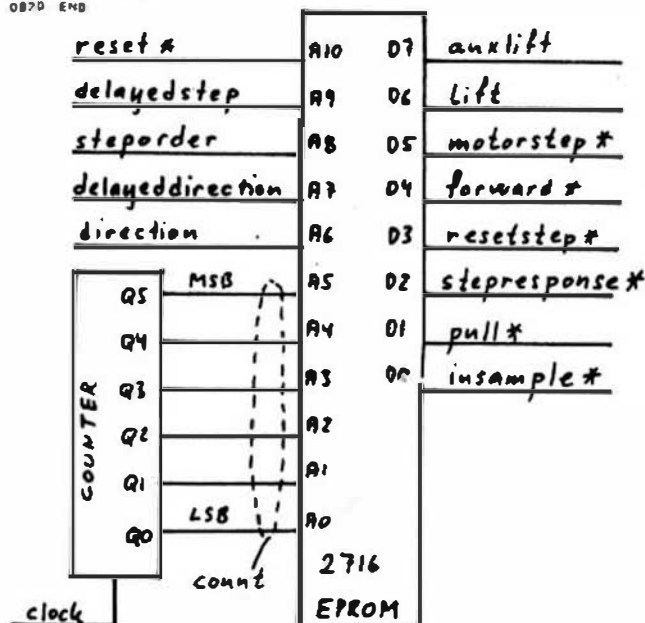
```



```

07CA IF delaystep THEN
07DB REM constant speed
07E4 motorstep=count+3 OR count=7 OR count=14 OR count=18
0804 motorstep=motorstep OR count=24 OR count=28 OR count=
35
0821 motorstep=delaystep OR count=39 OR count=46 OR count=
50
083E motorstep=motorstep OR count=56 OR count=60
0854 ELSE
0858 REM acceleration
0867 motorstep=count+6 OR count=22 OR count=38 OR count=46
08B7 motorstep=motorstep OR count=50 OR count=56 OR count=
60
08A4 ENDIF
08A6 ENDIF
08A8
08A9
08BC IF delaystep AND NOT(steporder) AND NOT(reset) THEN
08D3 REM delay the stepmotor
08D8 forward=delaydirection
08F8 motorstep=count+3 OR count=7 OR count=14 OR count=33
090A motorstep=motorstep OR count=39
090C ENDIF
090D
091C IF NOT(steporder) AND NOT(reset) THEN
0932 REM no steporder, lift:
0948 lift=TRUE
094F IF delaystep AND count=3 AND count=9 THEN
0955 auxlift=TRUE
0957 ENDIF
0959 ENDIF
095A
099A REM ===== transform the output condition to an eight bit byte:
099B
09B5 REM Assign the output bits:
09C1 B10:=UTtr.samples;
09C8 D11:=auxlift;
09D4 D12:=NOT(stepresponse);
09E3 D13:=NOT(resetstep);
09F1 D14:=NOT(forward);
09FD D15:=NOT(motorstep);
0A08 D16:=lift;
0A13 D17:=auxlift;
0A14
0A3A REM Initially, set all output bits low:
0A42 databyte=80H
0A43
0A73 REM Selectively, set the wanted output bits high:
0A8E REM in particular output bit
0A9E FOR I=0 TO 7
0AAC IF D11=TRUE THEN
0ABE databyte:=OR(databyte,2**I)
0AC0 ENDIF
0AC8 NEXT I
0ACC
0AF8 REM Write the byte to the EPROM pattern file:
0B02 PUT #file,databyte
0B03
0B2F REM Continue with the next input combination:
0B3A NEXT address
0B3B
0B73 REM ===== MAKE A NICE FINDING: =====
0B75 CLOSE #file
0B7D END

```



Drawing 1.

Computer Publishing Center
'68' Micro Journal
5900 Cassandra Smith Road
Hixon, Tennessee 37343

The Public Domain FLEX utilities I've been sending out, called the GIVEAWAY PACKAGE for the lack of a better name, has been updated. Several improvements have been made to CAT, COPY and DISKEDIT, often at the suggestion of Bob Jones. Several additions have been made, including a complete set of utilities for multivolume winchester drives using the WD-1000 or WD-1002-05 winchester controllers. The following catalog shows the dates of the current versions:

SQUEEZE .TXT	9-21-81	SAVE .TXT	2-03-82
WORDSWAP.TXT	3-06-82	DATE .TXT	4-04-82
LOWERCAS.TXT	5-23-82	DIRALL .TXT	5-23-82
CLEANUP .TXT	5-23-82	PICTURE .TXT	6-05-82
ALOAD .TXT	8-28-82	RESNORM.LIB	1-01-83
RESNORM.LIB	1-02-83	RESIDENT.TXT	1-02-83
RESIDENT.DOC	1-02-83	RESPROM.LIB	1-02-83
RESLBUGG.LIB	1-03-83	RESLBUGG.LIB	1-03-83
RAMBUG .LIB	5-04-83	FIND .TXT	10-10-83
FASTEXEC.TXT	2-07-84	COPY .DOC	2-09-84
PDEL .DOC	11-17-84	RECOVER .DOC	11-17-84
GEM .TXT	4-13-85	INITJOE .LIB	6-14-85
INITGAP .LIB	6-18-85	INITINFO.LIB	6-23-85
INITDRV .LIB	6-23-85	INIT .TXT	6-23-85
INITARL .LIB	7-19-85	RAMDISK .TXT	8-24-85
TEST .TXT	9-07-85	INITBOOT.LIB	9-17-85
DISKEDIT.TXT	9-17-85	DRIVERS .TXT	10-16-85
WINPARK .TXT	10-23-85	WINASN .TXT	10-24-85
DSKALIGN.TXT	10-29-85	DIRSIZE .TXT	11-16-85
WINTABLE.LIB	12-01-85	WINEXAM .DOC	12-04-85
WINDRV .TXT	12-08-85	WINFMT .TXT	12-08-85
WINBOOT .TXT	12-23-85	GEM .DOC	12-28-85
WIN .DOC	12-28-85	CAT .TXT	12-31-85
PROMPROG.TXT	1-04-86	CAT .DOC	1-11-86
PROMPROG.DOC	1-11-86	COPY .TXT	1-18-86
HEXCALC .TXT	2-03-86	DISKEDI2.TXT	3-16-86

Those who need most of the files updated, or have never sent for the GIVEAWAY package, can send me 6 five inch disks or 2 eight inch disks. Please include a stamped self addressed return container. You need not format the disks, I always record the disks SSD 35/77 tracks. Those who only need a few files updated can send me a list plus the number of formatted disks needed.

Alternately, the programs can be downloaded from Micheal Evenson's 680X Bulletin Board in California (213) 539-7619. You will need to make two calls a few days apart, the first call to establish your password which allows you access to the XMODEM (CP/M) download section.

Leo Taylor
109 Twin Brook Road
Hamden, Conn. 06514 USA

PERIPHERAL TECHNOLOGY

1480 Terrell Mill Rd., Suite 870
Marietta, Georgia 30067
Telex #880584

404/944-0742

PRODUCT ANNOUNCEMENT

COCO DRIVERS

PERIPHERAL TECHNOLOGY ANNOUNCES AVAILABILITY OF COCO COMPATIBLE DRIVERS FOR OS/9. THESE DRIVERS MAY BE LOADED BY THE USER AND ALLOW READING AND WRITING TO COCO FORMATTED OS/9 DISKETTES. EACH DRIVE TAKES ON A DUAL PERSONALITY AFTER THE DRIVERS ARE LOADED ALLOWING THE DRIVES TO RESPOND AS EITHER /DD OR /CO, /OI OR /CI ETC. THIS ALLOWS EASY DISKETTE INTERCHANGE BETWEEN USERS HAVING A COCO AND A P169 COMPUTER.

USE OF THE DRIVERS ON P169 COMPUTERS THAT DO NOT HAVE THE "MICROWARE STANDARD DISK FORMAT OPTION" WILL REQUIRE MODIFICATION OF THE P169 COMPUTER AND A NEW BOOT EPROM AND OS/9 SYSTEM DISKETTE. THESE DRIVERS ARE NOW INCLUDED WITH ALL NEW ORDERS FOR OS/9 OR SYSTEMS WITH OS/9. AN UPGRADE PACKAGE IS AVAILABLE FOR USERS WISHING TO UPGRADE THEIR P169 COMPUTER FOR COCO COMPATIBILITY. THE COST OF THIS PACKAGE IS \$30. MODIFICATION OF THE USER'S P169 IS AVAILABLE FOR AN ADDITIONAL \$15 IF THE USER DOES NOT WISH TO MODIFY THE BOARD HIMSELF.

FOR ADDITIONAL INFORMATION, PLEASE CONTACT:

PERIPHERAL TECHNOLOGY
1480 TERRELL MILL AD, SUITE B70
MAARIETTA, GA 30067
800/704-0742

NOTE: AFTER MODIFYING A P169 COMPUTER FOR THE NEW FORMAT YOU WILL ONLY BE ABLE TO READ YOUR OLD DISKETTES THAT WERE FORMATTED AS SINGLE SIDED/SINGLE DENSITY DISKETTES.

184 Mont Albert Ad.
Canterbury 3126
Australia.
Merch 17th 1986

Mr. Don Williams
68 Micro Journal,
5900 Cascoonda Smith Rd,
Hixson, TN 37343
U.S.A.

Dear Don,

I have just upgraded my home biased system to run a 68009 processor at 2.5 Mhz. I slow the processor down for all addresses above \$E000, by using a MMV to stretch phase two of the clock. This stretching of the clock allowed the use of the waiting, slower, monitor and I/O devices.

The system has two five inch and two eight inch disk drives and the increase in speed allows double density disk operation for both disk drives using program I/O (not DMA).

The five disk drives and the disk boot had to be altered, as so did the disk formatter program.

Whilst working on this upgrade I became very conscious of the number of disk sectors and the interleave factor used by Flex and of course I made good use of the Disk Sector Interleave article by Leo Taylor in the December 1985 issue of Micro Journal.

I still have to settle on the number of disk sectors and the interleave factor that I will finally use.

The attached program is a basic program that I wrote to compute the disk sector interleave and eliminate the tedious, pencil and paper task of working out of the numbers.

I have often used programs from Micro Journal and would like to contribute this program for publication, as I think it may be of use to others.

Many thanks for a good 68xx magazine.

Yours faithfully,

Howard Wills

Howard Wills.

DISK SECTOR INTERLEAVE BASIC PROGRAM

```
10 REM DISK SECTOR INTERLEAVE
20 REM
30 REM HOWARD WILLS      16/03/86
40 REM
50 REM VERSION 1.0      16/03/86
60 REM
70 REM THIS PROGRAM CALCULATES THE DISK SECTOR NUMBER
80 REM SEQUENCE FOR A GIVEN INTERLEAVE FACTOR & REPORTS
  ERRORS
90 REM
100 DIM S(99)
110 REM PRINT HEADER INFORMATION
120 GOSUB 640
130 REM PRINT SECTOR INFORMATION
140 GOSUB 710
150 REM GET REQUIRED SECTOR NUMBER
160 GOSUB 820
170 IF N>99 THEN 160
180 REM GET REQUIRED INTERLEAVE FACTOR
190 GOSUB 880
200 IF I>=N THEN 190
210 FOR A=1 TO N
220 S(A)=0
230 NEXT A
240 A=1 : H=0 : SN=2
250 E=0
260 S(A)=1
270 REM NOW STEP TO INTERLEAVE
280 A=A+1
290 IF A<N+1 THEN 310
300 A=A-N
310 IF E<>0 THEN 610
320 IF S(A)<>0 THEN 570
330 S(A)=SN
340 SN=SN+1
```

```
350 IF SN<>N+1 THEN 280
400 REM PRINT SECTOR PATTERN
370 FOR Z=1 TO N STEP 18
380 X=Z
390 Y=Z+17
400 IF Y>N THEN Y=N
410 GOSUB 460
420 PRINT
430 NEXT Z
440 GOSUB 940
450 GOTO 150
460 PRINT
470 FOR A=X TO Y
480 IF A<10 THEN PRINT " ";A;
490 IF A>9 THEN PRINT A;
500 NEXT A
510 PRINT
520 FOR A=X TO Y
530 IF S(A)<10 THEN PRINT " ";S(A);
540 IF S(A)>9 THEN PRINT S(A);
550 NEXT A
560 RETURN
570 H=H+1
580 IF H=N THEN E=1
590 A=A+1
600 GOTO 310
610 PRINT
620 PRINT "*** BAD INTERLEAVE FACTOR - PROGRAM ABORTED ***"
630 GOTO 150
640 PRINT
650 PRINT TAB(5);"DISK SECTOR INTERLEAVE PROGRAM BY HOWARD WILLS"
660 PRINT TAB(5);"*****"
670 PRINT
680 PRINT"MAXIMUM NUMBER OF SECTORS ALLOWED = 99"
690 PRINT
700 RETURN
710 PRINT"NORMAL FLEX DISK SECTOR VALUES ARE "
720 PRINT
730 PRINT"5 INCH S.D. = 10"
740 PRINT
750 PRINT"5 INCH D.D. = 11"
760 PRINT
770 PRINT"8 INCH S.D. = 15"
780 PRINT
790 PRINT"8 INCH D.D. = 26"
800 PRINT
810 RETURN
820 PRINT
830 PRINT"ENTER REQUIRED SECTOR VALUE - ";
840 INPUT N
850 IF N<>0 THEN RETURN
860 PRINT"*** CAN'T HAVE ZERO SECTORS ***"
870 GOTO 820
880 PRINT
890 PRINT"ENTER REQUIRED INTERLEAVE NUMBER = ";
900 INPUT I
910 IF I<>0 THEN RETURN
920 PRINT"*** CAN'T HAVE ZERO INTERLEAVE ***"
930 GOTO 880
940 PRINT
950 PRINT"HERE WERE ";H;" SECTOR CLASHES"
960 PRINT
970 RETURN
```

WESTCHESTER Applied Business Systems, Inc
2 Pee Pond Lane, Briarcliff Manor, New York 10610

Dear Don, Larry and Tom,

Several Users have inquired as to the differences between IDMS levels I, II and III - and the new IDMS-IV system. I am sure you have received similar questions. Let me attempt to briefly highlight the differences and some of the advantages of the new system.

Before doing this, I'll restate the purpose of these systems: They are designed to allow users to structure, enter, retrieve, process and format data. The user views file data as a tabular listing, with column (field) headings and rows of records. Any field is a potential sort key, selection key, or match key to other files. Data fields may be selected, reordered, merged from other files, and reformatted on output. Records may be sorted, organized into subsets, and inserted into report forms. Up to three files may be linked as a relational database on report output. Many other features exist, but for now let's concentrate on the new IDMS-IV system.

First of all, IDMS-IV is a single, integrated program. Once invoked, all commands are in memory and instantly available. With old IDMS, the User would first invoke the nucleus, and then enter each command from the FLEX *** prompt. There is a few second delay while each command loads from disk. With IDMS-IV, the User enters commands from a "X" prompt and there is no delay.

IDMS-IV is designed to be "session oriented", that is! The User does most of his/her work without exiting to PLEX. For this reason, We've built in DIR, LIST, COPY, RENAME and DELETE utility commands and a text editor. The database CREATE and UPDATE utilities are also integral and execute instantly. The REPORT and GENERATE functions disappear with IDMS-IV and become integral to the command interpreter. For ad hoc reports the user simply enters the necessary processing statements and a "RUN" command.

IDMS .CTL files are replaced by enhanced .PRC process files. Processes may execute utility commands, process commands, other processes or themselves. Menus and prompts may be output to the screen, and commands or processes may be conditionally executed based on operator selection.

The heading, form, body and footing text blocks which surround the insert, link and main file records on reports are replaced by a single integrated form command. Record or field placement is a function of indicators placed in the form text. Forms may be coded in-line, or may reside in a separate file. Form files may be used by multiple processes.

Coding of output Page size, margins, etc. for each process is eliminated by user preset attributes for the terminal and printer. These are automatically invoked depending on the output routing, and may be overridden if required. IDMS-IV also supports cursor positioning, home and clear, highlighting, etc. as available on most terminals. Printer boldface, underlining, double width and italics are supported. Control codes may be output to select font sizes or to configure other printer or terminal options prior to report output.

IDMS-IV is a completely new architecture with many other features. The highly efficient code occupies slightly more space than the IDMS nucleus and GENERATE together, yet provides all functions. The new manual contains an alphabetically organized command reference section, where each command is explained and illustrated.

I've attached a comparison matrix for other IDMS attributes. Naturally, I used IDMS-IV to create and print the matrix. Specific capabilities are indicated with a "Yes" or "No", and some are noted with a "Mod", meaning "separate module" or a "Int" meaning "integral command". The latter implies that the function may be executed within a process.

Because of the implementation effort involved, We view IDMS-IV as a totally new system, and not an upgrade. It's \$350.00 list price is a bargain when one realizes that it is comparable to popular PC software selling for much more. We do offer a migration incentive (discount) to current IDMS, IDMS+, and IDMS level I, II and III users. These users may order IDMS-IV for \$250.00 with valid proof of purchase. Orders may be placed with Southeast Media, 390a Cassandra Smith, Hixson TN 37343.

Best Regards,

Bill Adams
Bill Adams

*** IDMS COMPARISON ***

ATTRIBUTE	IDMS-L1	IDMS-L2	IDMS-L3	IDMS-IV
Architectural: Modular/Integrated	Mod	Mod	Mod	Int
Number of modules	4	5	16	1
Position Independent Code	No	No	No	Yes
Relocatable	No	No	No	No
Session Oriented	No	No	No	Yes
Maximum Fields/Groups per Record	24	24	24	32
Maximum Label Characters	8	8	8	12
Maximum Record Size	256	256	256	1024
User Install Term/Print Attributes	No	No	No	Yes
Dynamic Set Output Attributes	Yes	Yes	Yes	Yes
Virtual Paging to Dedicated Disk	Yes	Yes	Yes	Yes
Virtual Paging to Random File	No	No	No	Yes
Terminal Cursor Control Support	No	No	No	Yes
Printer Special Feature Support	No	No	No	Yes
Process Control Files	Yes	Yes	Yes	Yes
Execute a Process from a Process	No	No	No	Yes
Operator Menu/Process Selection	No	No	No	Yes
Create, Update & List File	Yes	Yes	Yes	Yes
Maximum Record Selection Tests	15	15	15	15
Equal, Less, Greater Tests	Yes	Yes	Yes	Yes
Starts-with/Masked Tests	Yes	Yes	Yes	Yes
Contains-string Test	No	No	No	Yes
Not Starts-with/Contains Tests	No	No	No	Yes
Tests against other fields	No	No	No	Yes
Select Specific Fields for O/P	Yes	Yes	Yes	Yes
String Multiple Fields into One	No	No	No	Yes
Redefine field type/en on O/P	No	No	No	Yes
Merge fields from Auxiliary File	Yes	Yes	Yes	Yes
Join Records from Two Files	No	No	No	Yes
Array/classify data into columns	No	Yes	Yes	Yes
Sum records/arrays by key value	No	Yes	Yes	Yes
Un-array columns into records	No	No	No	Yes
Calculation on field data	Yes	Yes	Yes	Yes
Maximum Sort Fields	15	15	15	15
Insert File as Report Heading	No	Yes	Yes	Yes
Link Three Files as MAIN on O/P	No	Yes	Yes	Yes
Invert File Relationship on O/P	No	No	No	Yes
Insert Records within form text	No	Yes	Yes	Yes
Insert record fields into text	No	Yes	Yes	Yes
Integrated Forms & Form Files	No	No	No	Yes
Output report to File	No	Yes	Yes	Yes
Output to Database File	No	Yes	Yes	Yes
Output Database to ASCII File	No	No	Mod	Int
Input ASCII File to Database	No	No	Mod	Int
Purge Database File	No	No	Mod	Int
Plot (Bar Graph) Function	No	No	Mod	No
Display File Format	No	No	Mod	Int
General File Utilities	No	No	No	Yes
Text Editor	No	No	No	Yes

Micro Concepts launch new Microbox III at Microprocessor Development Show

Micro Concepts launch their new Microbox III - a British made competitor to the Commodore Amiga and the Atari ST520 - at the Microprocessor Development Show, Wembley Conference Centre, February 11-13. Micro Concepts are at 2 Stephens Road, Cheltenham, Glos, GL51 5AA, telephone (0242) 510525.

Microbox III is a low cost, versatile single board colour graphics computer, based on the fast operating 68000 processor. It is available as a complete system with power supply, disk drive, monitor and keyboard, with power supply and disk drives only, or as an assembled and tested board for OEM applications. Prices start at £650 + VAT, putting the Microbox III easily within reach of the personal computer user.

The system is based on a 720 x 230 mm eurocard, and contains 512k bytes of ram, up to 192k bytes of eeprom, medium resolution colour graphics and a wide variety of mass storage and communication peripherals. Special features include exceptional colour graphics with gen-locked video, interfaces for twin 800k byte floppy and 20 megabyte hard disks, up to 24k bytes of CMOS battery-backed static ram, a Smart real time clock, parallel and serial ports and a mouse interface - while the choice of operating systems includes TRIPDS, GEN (CPM 68k), DS9-68k and the QDOS-compatible SMS-2. GEN and TRIPDS are compatible, respectively, with the Atari and Commodore systems. Software in the form of systems services and a WIMP type user interface is provided as standard.

Unlike the American systems, it is designed to use the PAL video standard (though the NTSC standard can be used) giving higher screen resolution and proper gen-locking circuitry. Microbox III also has a higher bus band width: 90 - 100% compared with 5 -

100% for the Amiga, and it has a wider choice of display modes than either machine.

The main memory is provided by 16 256k bit d-rams, giving 512k bytes - shared between the processor (running at 8 MHz for 90% of the time) and the display, using an interleaved scheme which gives the processor access to the ram at any time without disturbing the display. The display uses 80k bytes, leaving 432k bytes available. Two areas of battery-backed CMOS static ram are also provided, holding up to 24k bytes and with a battery life of up to 10 years; one is combined with the eeprom socket, the other with the real time clock. The latter can hold system parameters - character sets etc., and is protected against system crashes.

The four 28 pin eeprom sockets can hold up to 192k bytes of eeprom. Two sockets may be populated with 27 512 eeproms, with 128k bytes of system software. The remaining two can be configured either for two 27256 eeproms or, with the addition of two Smart sockets, two 8k or 32k CMOS static ram. By changing links these two sockets can also be configured to be an on-board 27256 eeprom programmer, allowing the board to act as a stand-alone development system.

Display is based on the Motorola Senter Management System chip set, giving either 80 x 25 text with near definable character sets, or up to 640 x 500 with 4 colours or 320 x 215 with 16 colours. Look up tables give 32 colours out of a range of 4096, on display at any one time. Both vertical and horizontal smooth scrolling is available, and the video can be gen-locked or synchronized to an incoming composite video input, allowing the board's graphic output to be mixed or overlaid with the incoming video. Other features include a dual 5 1/4" or 3 1/2" floppy disk drive interface, using the Western Digital 1772 device and giving a total of 800k bytes on a single drive, or 1.6 megabytes for the whole system. There is also a SASI bus interface to connect to a 3 1/2" 20 megabyte Winchester disk drive.

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SPERRY NEWS

Introduces Two High-Performance 32-Bit Series 5000 Systems

BLUE BELL, PA — Sperry introduced two new members of the Series 5000 family of microprocessors utilizing the UNIX[®] operating system - the Model

50 and the Model 90.

Broadening Sperry's micro-to-mainframe product line supporting the UNIX OS, the new systems utilize 32-bit MC68020[™] technology and offer improved performance over existing Series 5000 models.

The 5000/50 and 5000/90 offer full 32-bit capability with CPU performance over two times their Series 5000 predecessors. Utilizing an optimized UNIX System V operating system and C compiler for the MC68020, both systems are functionally compatible with other Series 5000 members. Users can move applications, horizontal software tools, programming languages and interconnect software across systems without recompilation.

Both systems provide a common interface to industry standard software, peripherals and communications facilities supported by other Series 5000 products. The systems function as stand-alone or departmental systems supporting SNA, X.25, Ethernet[®] and other industry standard data communications protocols. The industry standard design enables users to maximize hardware investment and remain flexible when reconfiguring or enhancing systems.

In addition to the new models, Sperry announced upgrade capability for existing Series 5000 systems, Models 40, 60 and 80, introduced in November, 1984. The earlier models may be field-upgraded through installation of the 32-bit MC68020 CPU and a revised operating system.

Pricing and Availability

The Series 5000/50 basic hardware ranges in price from \$23,030 to \$28,530 and is currently available. Basic Series 5000/90 hardware ranges in price from \$68,300 to \$74,300 and will be available in June, 1986. System options, workstations and software licensing fees are priced separately.

MC68020 field upgrade capability for existing Series 5000/40, 5000/60 and 5000/80 range in price from \$6,995 to \$12,000 and will be available in July, 1986.

All products are sold through Sperry's worldwide sales organization and authorized Sperry dealers.

Sperry Series 5000, Model 50

The Series 5000/50 can support up to 32 interactive users. The CPU with 8 kilobytes (KB) of data and program cache memory and 2 to 16 megabytes (MB) of main memory (RAM). Improves processing performance and allows the execution of large, complex programs. An optional MC68881 Floating Point Processor can be added.

A minimum configuration includes a 68020 Processor, 8 KB cache memory, 2 MB main memory, 85 MB fixed disk, 45 MB streaming cartridge tape, 4 async RS-232 ports, 2 synchronous ports, 1 parallel port, sync line interface module and power supply with battery back-up.

The 5000/50 supports up to two expansion cabinets. One Small Computer System Interface (SCSI) tape drive controller and one 1600/3200 bpi tape drive are standard with each cabinet. A 10 Mhz disk drive controller and up to two 340 MB fixed disk drives are optional, enabling the 5000/50 to grow to a maximum system capacity of 1.6 gigabytes (GB).

Sperry Series 5000, Model 90

The Series 5000/90 can support up to 88 interactive users and features the ability to install up to four 68020 processors for expansion. Memory ranges from 4 to 16 MB and the system supports 8 KB of data and program cache memory.

A MC68001 Floating Point Processor is standard. This processor permits hardware acceleration of mathematical calculations.

A 5000/90 minimum configuration includes a 68020 processor, Floating Point Processor, 8 KB cache memory, 4 MB main memory, 160 MB fixed disk, 45 MB streaming cartridge tape, 8-channel Direct Memory Access (DMA) controller, 16 sync/asnc ports, 2 parallel ports and power supply.

The 4-port DMA Controller allows attachment of four disk/tape controllers permitting a maximum of sixteen disks and eight tapes to be configured. Disk types range from 160 MB (processor cabinet only) to 515 MB drives (expansion cabinet only). Up to four expansion cabinets are permitted for a maximum capacity of up to 9 gigabytes (GB).

Sperry's UNIX OS Product Line

Sperry's micro-to-mainframe family of Personal Computers, 5000 Series of multi-user microcomputers, the Sperry 7000/40 super minicomputer and the Sperry 1100 Series offer the industry's largest range of computing power based on AT&T's UNIX System V Operating System. The UNIX OS compatibility allows orderly system growth, protects hardware and software investment and provides unparalleled applications portability — from the desk-top all the way to the computer room.

Sperry is a leading manufacturer and supplier of electronics-based, high-technology systems and services for commercial business and government, defense, aerospace and maritime markets. Sperry's computer operations serve more than 18,000 customers in 50 countries and, in fiscal year 1985, reported revenue of \$4.15 billion, part of a total corporate revenue of \$5.7 billion.

RELEASE NO: 486/3259

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M68000 MICRO MINUTES

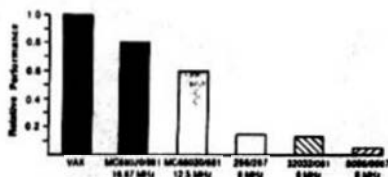
MM- 551-02

REAL-LIFE PERFORMANCE OF THE MC68001

Now that several third party software vendors have had a chance to optimize their Fortran compilers to produce in-line MC68001 object code (versus either subroutine or trap calls), we thought it might be interesting to once again perform some Whetstone comparisons between these compilers and other machines. The following table encapsulates the results, and proves conclusively that the MC68001 delivers the best floating point performance of any microprocessor implementation!

Configuration/Ref	Processor/Compiler	Speed (MIPS)	Whetstone
VAX 11/780 (FPA)	VMS/DEC Fortran	18.67	1,250
MINI 3 (050881)	4 2nd/177 rel 3.1	18.67	1,250
MC68000/81 (BM20)†	Unisoft Unix™ V/VS53	12.5	760
MC68000/81 (BM20)	Unisoft Unix™ V/VS53	8.0	193
80286/80287 (310)‡	Xerox/Intel Fortran	8.0	193
NS32032/081§		8.0	193
8096/8087 (310)		8.0	63

1. Floating Point Accelerator (board set \$14K)
2. Motorola "Benchmark 20"
3. Silicon Valley Software Optimized Fortran Compiler
4. Intel 286/316-41ES ("Engineering Special")
5. Hardware/System/Compiler unknown — from published material by National



MOTOROLA
Austin, Texas

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MC68001 PERFORMANCE



MUSTANG-020 & UniFLEX 6809/68020 X-TALK A C-Modem/Hardware Hookup

Exclusive for UniFLEX ~~MUSTANG~~-020 is a new package from Data Comp (CPI). X-TALK consists of two disks and a special cable, the hookup enables a 6809 SWTPC computer to dump UniFLEX files directly to the UniFLEX ~~MUSTANG~~-020. This is the **ONLY** currently available method to transfer SWTP 6809 UniFLEX files to a 68000 UniFLEX system. Cimix 6809 users may dump a 6809 UniFLEX file to a 6809 UniFLEX five inch disk and it is readable by the ~~MUSTANG~~-020.

The cable is specially prepared with internal connections to match the non-standard SWTPC S0/9 I/O Db25 connectors. A special SWTPC S+ cable set is also available. Users should specify which SWTPC system he/she wishes to communicate with the ~~MUSTANG~~-020.

The X-TALK software is furnished on two disks. One eight inch disk contains the S.E. MEDIA modem program C-MODEM (6809) the other disk is a ~~MUSTANG~~-020 five inch disk with C-MODEM (68020). Text and binary files may be directly transferred between the two systems. The C-MODEM programs are unaltered and perform as excellent modem programs also.

X-TALK can be purchased with or without the special cables, but this special price is available to **registered** ~~MUSTANG~~-020 users only

X-TALK Complete (cable, 2 disks)	\$99.95
X-TALK Software (2 disk only)	\$69.95
X-TALK with C-MODEM Source Included	\$149.95

Order from:

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Almond, TN 37343
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TELEX 510 600-6630

Note: ~~MUSTANG~~-020 current owners must furnish serial number from back plate of ~~MUSTANG~~-020 system for this special offer.

MICRONICS
RESEARCH CORP.

Dear Don,

Last time I wrote, I almost got side-tracked into a discussion of the INT(X) function, which in turn would have led me on to Integer Variables. You may wonder what I could possibly say about these that you don't already know, but I'll have a go at it anyway.

To begin with, let's agree that the INT of a non-integer Floating-Point number is the integer immediately **BELOW** that number. That is to say, INT(5.7) = 5 and INT(-5.7) = -6. It is unfortunate that the KBASIC compiler (not **KBASIC**) has chosen to change this definition for negative numbers, thus making their INT(X) into a TRUNCATE(X). To continue with our discussion, the numbers 1, 13, -15, etc are Integer constants, while AX, BX, and CX are Integer Variables in the range +/- 32767, and A, B and C are Floating-Point variables (FP variables, for short).

OK, now let's get down to some serious business. You'll find that lots of programs can be speeded up (quite apart from taking up less room in memory) if you make as many variables as possible into Integers.

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As a case in point, let's consider the simple loop :

```
10 FOR I = 1 TO 10
20 PRINT I;
30 NEXT I
```

RUNning this program will produce the following :

```
1 2 3 4 5 6 7 8 9 10
```

If the 'I's are changed to 'IX', the result will be the same, only it will happen faster.

Now let's add another line to the original program, and RUN it again.

```
25 IF I/3 = INT(I/3) THEN PRINT "BOING!";
```

This time we'll see

```
1 2 3 BOING! 4 5 6 BOING! 7 8 9 BOING! 10
```

but not if we change all 'I's to 'IX' as we did for the first example. This time we'll see 'BOING!' printed out after each and every number. What went wrong??

If we look at I/3 and INT(I/3) for the first program, we have

I	1	2	3	4	5	6	7	etc
I/3	.33	.66	1	1.33	1.66	2	2.33	etc
INT(I/3)	0	0	1	1	1	2	2	etc

causing a match at every '1' which is exactly divisible by 3, whereas IX/3 and INT(IX/3) are both identical to the line for INT(I/3) above. How can we preserve the intent of the original program, and STILL change our 'I's to 'IX'? If we keep in mind that IX/3 produces the sequence 0,0,1,1,1,2 only because IX and 3 are both Integers, the solution is to make one of them a Floating-Point Integer, which will produce a FP result. We obviously can't do this with IX, but we can change the '3' to '3.' (the added decimal-point indicating that '3' is really a FP '3.00') to make Line 25 IF IX/3. = INT(IX/3) THEN PRINT "BOING!"; and we've achieved the desired result. Of course, an astute reader would also observe that we no longer need the INT() part either, so line 25 ends up as

```
25 IF IX/3. = IX/3 THEN PRINT "BOING!";
```

Another candidate for conversion is the pattern :

```
X = INT(RND(0) * 52 + 1)
```

which selects a random integer in the range 1 - 52, as part of a card-shuffling routine, let's say.

We simply change this to read XI = RND(0) * 52 + 1.

But there are many pitfalls awaiting the unwary - especially where division is involved (as in our first example) or if we venture into the domain of negative numbers. Also what do we do, if instead of IX/3 (which was easy to change to IX/3.) we have the situation IX/JX, where it is impossible to tack a decimal-point onto either Integer??

Let's examine these different possibilities. Suppose we consider one line of a program :

```
100 A = INT(B / 4 * C)
```

where examination of the complete program shows that A, B, and C are always integers. A prime candidate for conversion to AX, BX, and CX (and elimination of INT) you'd think. But if we assign, let's say, the values B = 7 and C = 5 then Line 100 as given would produce the result A = 8, because INT(7 / 4 * 5) = INT(8.75) = 8. On the other hand AX = BX / 4 * CX would give the result as 5. (Why?) Changing the '4' to '4.' as above produces the correct result of 8.

But what if we were to replace the constant '4' in our Line 100 with the Variable D, and assign the value 4 to D? It makes no difference to Line 100 as it stands, but in our transformed Line we would have

```
AX = BX / DX * CX
```

which would again give the wrong result of 5. What to do? We now have nowhere to tack on a decimal-point!!

A quick and dirty solution is to change the order of the variables on the right-hand side of the equation to give AX = BX * CX / DX (try it, and compare), where division is now the last operation to be carried out. This, however, will only work if the partial product, BX * CX, does not exceed the range +/- 32767, and provided the end result is non-negative. Try setting B = -7, and compare with the case of BX = -7.

A more elegant solution would be to preserve the order of the variables, but to multiply the first variable on the right-hand side by the identity for multiplication. This is equal to '1' (or '1.' in our example) as multiplying (or dividing) a number by '1' leaves it unchanged, i.e. it preserves its identity. Similarly the identity for addition (or subtraction) equals '0', as adding 0 to (or subtracting it from) a number leaves the number unchanged. Now we have

```
AX = BX * 1. / DX * CX
```

which should satisfy the transformation. On the other hand, as addition is faster than multiplication it would make more sense to write it as

```
AX = (BX + 0.) / DX * CX
```

Well, who would have thought there was so much to write about INTEGERS? There's no doubt that I've overlooked a few problem areas somewhere, but this discussion should at least pinpoint some of them and perhaps offer some guidelines for overcoming them. So tread warily when you venture into the field of Integer-Variables and the INT() function - don't make any assumptions as to what the result will be, but test your assignments and expressions for a range of conditions before making them permanent.

At this point, I'm not sure what I'll talk about next time as I seem to have run out of steam on X BASIC. However, we'll see!

Sincerely,

Bob

R. Jones
33383 LYNN AVENUE,
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OS-9 UniFLEX MUSTANG-020, 68020, 68881 AND MORE HANDS-ON EXPERIENCE

The DATA-Comp Division of Computer Publishing Corporation announces their new and innovative HANDS-ON 68020 computer familiarization two day event. A chance to TRY BEFORE YOU BUY!

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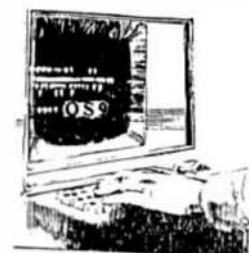


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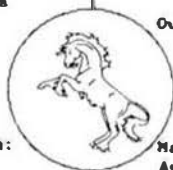
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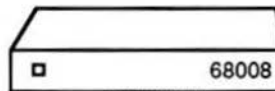
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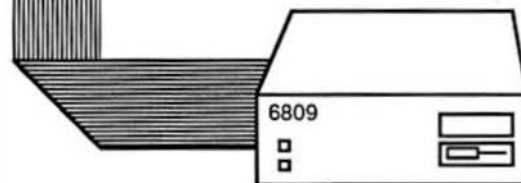
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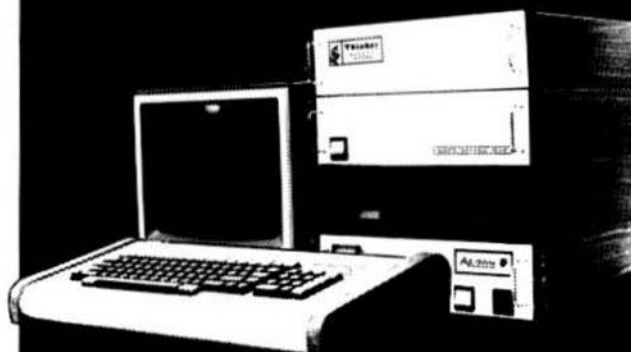
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PT-69 SINGLE BOARD COMPUTER SYSTEMS

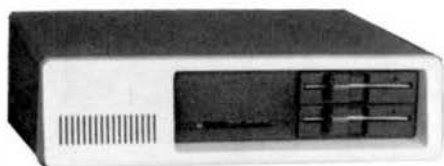
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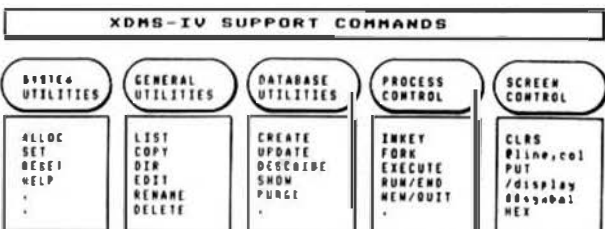
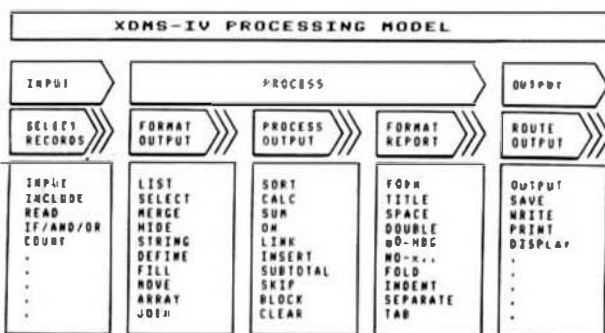
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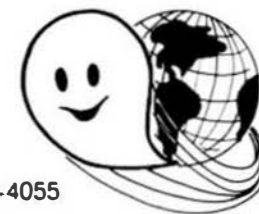
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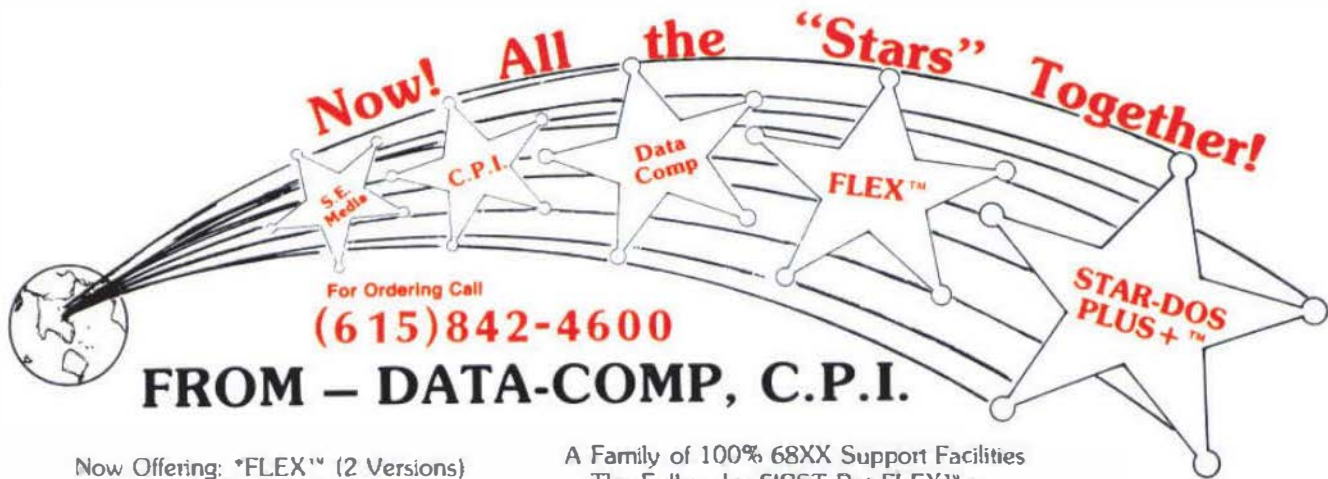
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